# TJA1057

## High-speed CAN transceiver

Rev. 6 — 24 August 2017 Product data sheet

## 1. General description

The TJA1057 is part of the Mantis family of high-speed CAN transceivers. It provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1057 offers a feature set optimized for 12 V automotive applications, with significant improvements over first- and second-generation CAN transceivers from NXP, such as the TJA1050, and excellent ElectroMagnetic Compatibility (EMC) performance. The TJA1057 also displays ideal passive behavior to the CAN bus when the supply voltage is off.

A $V_{IO}$ pin on the TJA1057GT(K)/3 variants allows for direct interfacing with 3.3 V and 5 V-supplied microcontrollers.

The TJA1057 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. The TJA1057T is specified for data rates up to 1 Mbit/s. Additional timing parameters defining loop delay symmetry are specified for the other variants. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

These features make the TJA1057 an excellent choice for HS-CAN networks that only require basic CAN functionality.

## 2. Features and benefits

### 2.1 General

- Fully ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant
- Optimized for use in 12 V automotive systems
- EMC performance satisfies 'Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications', Version 1.3, May 2012.
- $V_{IO}$ input on TJA1057x/3 variants allows for direct interfacing with 3 V to 5 V microcontrollers. Variants without a $V_{IO}$ pin can interface with 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.
- AEC-Q100 qualified
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- Both $V_{IO}$ and non-$V_{IO}$ variants are available in SO8 and leadless HVSON8 (3.0 mm $\times$ 3.0 mm) packages; HVSON8 with improved Automated Optical Inspection (AOI) capability.

### 2.2 Predictable and fail-safe behavior

- Functional behavior predictable under all supply conditions
- Transceiver disengages from bus when not powered (zero load)
- Transmit Data (TXD) dominant time-out function
- Internal biasing of TXD and S input pins

### 2.3 Protection

- High ESD handling capability on the bus pins (8 kV IEC and HBM)
- Bus pins protected against transients in automotive environments
- Undervoltage detection on pins $V_{CC}$ and $V_{IO}$
- Thermally protected

### 2.4 TJA1057 CAN FD (applicable to all product variants except TJA1057T)

- Timing guaranteed for data rates up to 5 Mbit/s
- Improved TXD to RXD propagation delay of 210 ns

## 3. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 4.75 | - | 5.25 | V |
| $V_{IO}$ | supply voltage on pin $V_{IO}$ | | 2.95 | - | 5.25 | V |
| $V_{uvd(VCC)}$ | undervoltage detection voltage on pin $V_{CC}$ | | 3.5 | 4 | 4.3 | V |
| $V_{uvd(VIO)}$ | undervoltage detection voltage on pin $V_{IO}$ | | 2.1 | - | 2.8 | V |
| $I_{CC}$ | supply current | Silent mode | 0.1 | - | 1.2 | mA |
| | | Normal mode; bus recessive | 2 | 5 | 10 | mA |
| | | Normal mode; bus dominant | 20 | 45 | 70 | mA |
| $I_{IO}$ | supply current on pin $V_{IO}$ | Silent mode | - | 3 | 16 | µA |
| | | Normal mode | | | | |
| | | recessive; $V_{TXD} = V_{IO}$ | - | 7 | 30 | µA |
| | | dominant; $V_{TXD} = 0$ V | - | 110 | 320 | µA |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 at pins CANH and CANL | –8 | - | +8 | kV |
| $V_{CANH}$ | voltage on pin CANH | limiting value according to IEC60134 | –42 | - | +42 | V |
| $V_{CANL}$ | voltage on pin CANL | limiting value according to IEC60134 | –42 | - | +42 | V |
| $T_{vj}$ | virtual junction temperature | | –40 | - | +150 | °C |

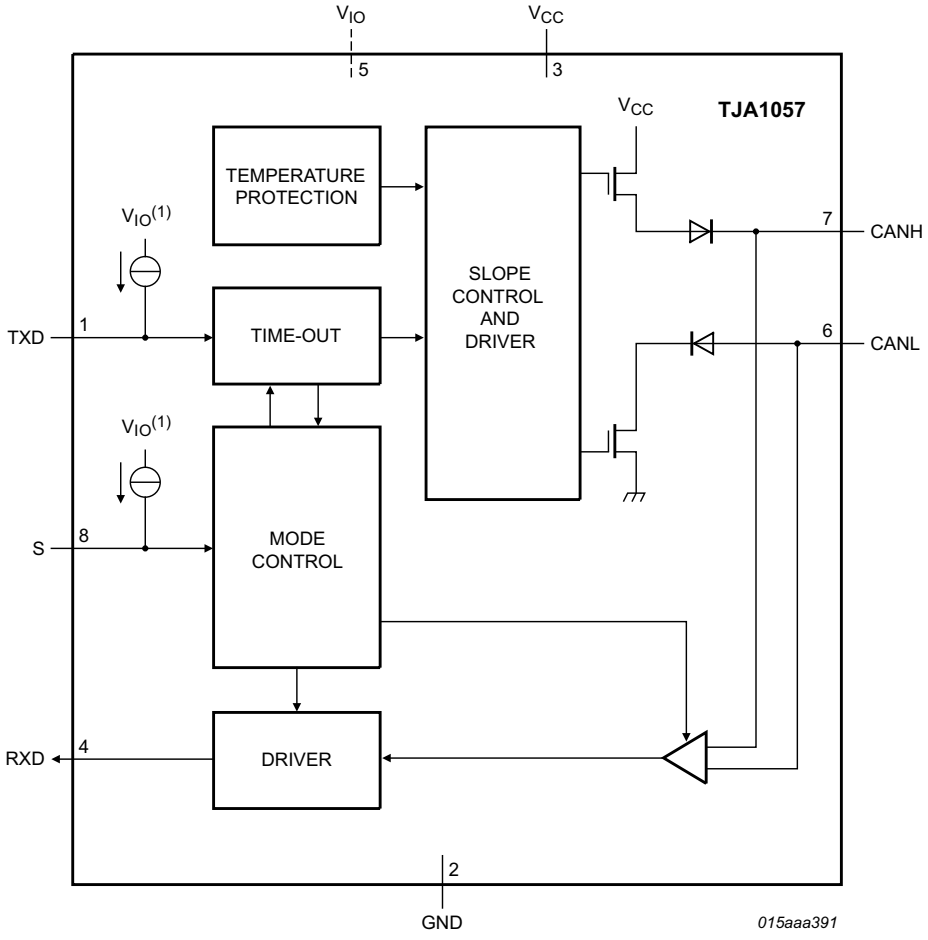
# 4. Ordering information

**Table 2. Ordering information**

| Type number[1] | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TJA1057T<br>TJA1057GT<br>TJA1057GT/3 | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| TJA1057GTK<br>TJA1057GTK/3 | HVSON8 | plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm | SOT782-1 |

[1] TJA1057GT/3 and TJA1057GTK/3 with $V_{IO}$ pin; all variants other than TJA1057T support CAN FD.

# 5. Block diagram

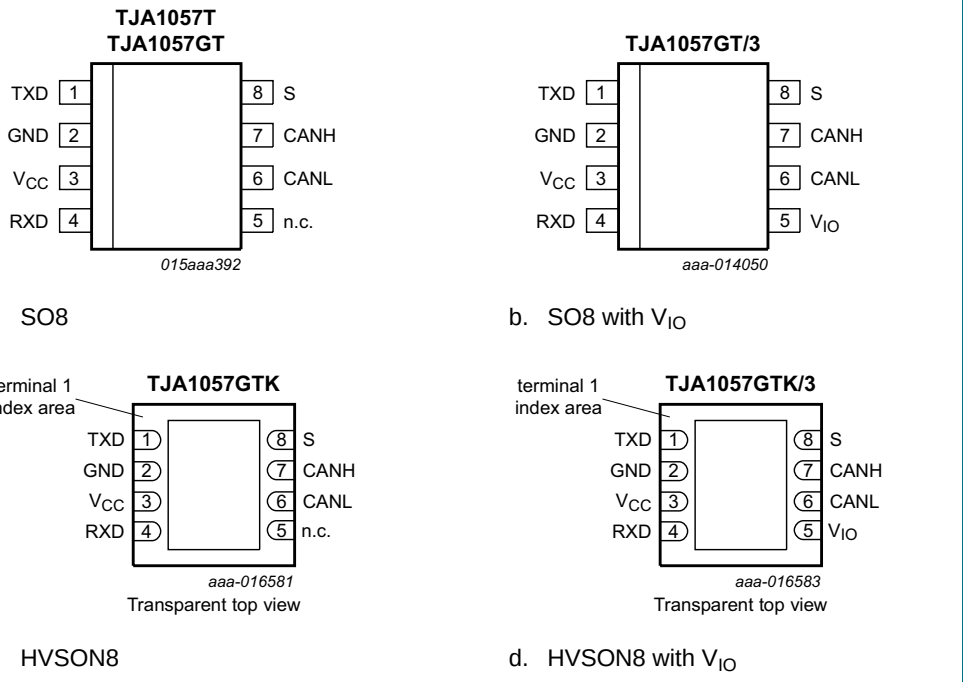



(1) $V_{IO} = V_{CC}$ in non-$V_{IO}$ product variants.

**Fig 1. Block diagram**

# 6. Pinning information

## 6.1 Pinning




a. SO8

b. SO8 with $V_{IO}$

c. HVSON8

d. HVSON8 with $V_{IO}$

**Fig 2. Pin configuration diagrams**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| TXD | 1 | transmit data input |
| GND[1] | 2 | ground |
| $V_{CC}$ | 3 | supply voltage |
| RXD | 4 | receive data output; reads out data from the bus lines |
| n.c. | 5 | not connected in TJA1057T, TJA1057GT and TJA1057GTK |
| $V_{IO}$ | 5 | supply voltage for I/O level adapter in TJA1057GT/3 and TJA1057GTK/3 |
| CANL | 6 | LOW-level CAN bus line |
| CANH | 7 | HIGH-level CAN bus line |
| S | 8 | Silent mode control input |

[1] HVSON8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

# 7. Functional description

## 7.1 Operating modes

The TJA1057 supports two operating modes, Normal and Silent. The operating mode is selected via pin S. See Table 4 for a description of the operating modes under normal supply conditions.

**Table 4. Operating modes**

| Mode | Inputs | | Outputs | |
|---|---|---|---|---|
| | Pin S | Pin TXD | CAN driver | Pin RXD |
| Normal | LOW | LOW | dominant | LOW |
| | | HIGH | recessive | LOW when bus dominant |
| | | | | HIGH when bus recessive |
| Silent | HIGH | x[1] | biased to recessive | LOW when bus dominant |
| | | | | HIGH when bus recessive |

[1] ‘x’ = don’t care.

### 7.1.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines, CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

### 7.1.2 Silent mode

A HIGH level on pin S selects Silent mode. The transmitter is disabled in Silent mode, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller disrupting all network communications.

## 7.2 Fail-safe features

### 7.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of approximately 25 kbit/s.

### 7.2.2 Internal biasing of TXD and S input pins

Pins TXD and S have internal pull-ups to $V_{CC}$ (or $V_{IO}$ in TJA1057GT(K)/3 variants) to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Silent mode to minimize supply current.

### 7.2.3 Undervoltage detection on pins $V_{CC}$ and $V_{IO}$ (TJA1057GT(K)/3)

If $V_{CC}$ or $V_{IO}$ drops below the undervoltage detection level, $V_{uvd(VCC)}$/$V_{uvd(VIO)}$, the transceiver switches off and disengages from the bus (zero load; bus pins floating) until the supply voltage has recovered. The output drivers are enabled once both $V_{CC}$ and $V_{IO}$ are again within their operating ranges and TXD has been reset to HIGH.

### 7.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, both output drivers are disabled. When the virtual junction temperature drops below $T_{j(sd)}$ again, the output drivers recover once TXD has been reset to HIGH (waiting for TXD to go HIGH prevents output driver oscillation due to small variations in temperature).

### 7.2.5 $V_{IO}$ supply pin (TJA1057x/3 variants)

Pin $V_{IO}$ should be connected to the microcontroller supply voltage (see Figure 6). The signal levels on pins TXD, RXD and S will then be adjusted to the I/O levels of the microcontroller, allowing for direct interfacing without additional glue logic.

For versions of the TJA1057 without a $V_{IO}$ pin, the $V_{IO}$ input is internally connected to $V_{CC}$. The signal levels of pins TXD, RXD and S are set to levels compatible with 5 V microcontrollers.

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_x$ | voltage on pin x[1] | on pins CANH, CANL | –42 | +42 | V |
| | | on pins $V_{CC}$, $V_{IO}$ | –0.3 | +7 | V |
| | | on any other pin [2] | –0.3 | $V_{IO}$[3] + 0.3 | V |
| $V_{(CANH-CANL)}$ | voltage between pin CANH and pin CANL | | –27 | +27 | V |
| $V_{trt}$ | transient voltage | on pins CANH, CANL [4] | | | |
| | | pulse 1 | –100 | - | V |
| | | pulse 2a | - | 75 | V |
| | | pulse 3a | –150 | - | V |
| | | pulse 3b | - | 100 | V |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 (150 pF, 330 Ω) [5] | | | |
| | | on pins CANH and CANL | –8 | +8 | kV |
| | | Human Body Model (HBM); 100 pF, 1.5 kΩ [6] | | | |
| | | on pins CANH and CANL | –8 | +8 | kV |
| | | on any other pin | –4 | +4 | kV |
| | | Machine Model (MM); 200 pF, 0.75 μH, 10 Ω [7] | | | |
| | | on any pin | –200 | +200 | V |
| | | Charged Device Model (CDM); field Induced charge; 4 pF [8] | | | |
| | | on corner pins | –750 | +750 | V |
| | | on any other pin | –500 | +500 | V |
| $T_{vj}$ | virtual junction temperature | [9] | –40 | +150 | °C |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] Maximum voltage should never exceed 7 V.

[3] $V_{IO} + 0.3 = V_{CC} + 0.3$ in the non-$V_{IO}$ product variants TJA1057(G)T(K).

[4] According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

[5] According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.

[6] According to AEC-Q100-002.

[7] According to AEC-Q100-003.

[8] According to AEC-Q100-011; grade C4B.

[9] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of $T_{vj}$. The rating for $T_{vj}$ limits the allowable combinations of power dissipation (P) and ambient temperature ($T_{amb}$).

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

*According to IEC 60747-1.*

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th(vj-a)}$ | thermal resistance from virtual junction to ambient | SO8 package; in free air | 97 | K/W |
| | | HVSON8 package; in free air | | |
| | | dual-layer board [1] | 91 | K/W |
| | | four-layer board [2] | 52 | K/W |

[1] According to JEDEC JESD51-2, JESD51-3 and JESD51-5 at natural convection on 1s board with thermal via array under the exposed pad connected to the second copper layer.

[2] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer.

# 10. Static characteristics

**Table 7. Static characteristics**

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.75 V to 5.25 V; $V_{IO}$ = 2.95 V to 5.25 V [1]; $R_L$ = 60 Ω; $C_L$ = 100 pF unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC. [2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply; pin $V_{CC}$** | | | | | | |
| $V_{CC}$ | supply voltage | | 4.75 | - | 5.25 | V |
| $V_{uvd(VCC)}$ | undervoltage detection voltage on pin $V_{CC}$ | | 3.5 | 4 | 4.3 | V |
| $I_{CC}$ | supply current | Silent mode; $V_{TXD} = V_{IO}$ [3] | 0.1 | - | 1.2 | mA |
| | | Normal mode | | | | |
| | | recessive; $V_{TXD} = V_{IO}$ [3] | 2 | 5 | 10 | mA |
| | | dominant; $V_{TXD}$ = 0 V | 20 | 45 | 70 | mA |
| | | dominant; short circuit on bus lines; $V_{TXD}$ = 0 V; −3 V < ($V_{CANH} = V_{CANL}$) < +18 V | 2 | 80 | 110 | mA |
| **I/O level adapter supply; pin $V_{IO}$ [1]** | | | | | | |
| $V_{IO}$ | supply voltage on pin $V_{IO}$ | | 2.95 | - | 5.25 | V |
| $V_{uvd(VIO)}$ | undervoltage detection voltage on pin $V_{IO}$ | | 2.1 | - | 2.8 | V |
| $I_{IO}$ | supply current on pin $V_{IO}$ | Silent mode | - | 3 | 16 | μA |
| | | Normal mode | | | | |
| | | recessive; $V_{TXD} = V_{IO}$ [3] | - | 7 | 30 | μA |
| | | dominant; $V_{TXD}$ = 0 V | - | 110 | 320 | μA |
| **Silent mode control input; pin S** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2 | - | $V_{IO}$ [3] + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | 0.8 | V |
| $I_{IH}$ | HIGH-level input current | $V_S = V_{IO}$ [3] | −1 | - | +1 | μA |
| $I_{IL}$ | LOW-level input current | $V_S$ = 0 V | −15 | - | −1 | μA |

**Table 7. Static characteristics** *…continued*

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.75 V to 5.25 V; $V_{IO}$ = 2.95 V to 5.25 V[1]; $R_L$ = 60 Ω; $C_L$ = 100 pF unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC.[2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CAN transmit data input; pin TXD** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2 | - | $V_{IO}$[3] + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | 0.8 | V |
| $I_{IH}$ | HIGH-level input current | $V_{TXD} = V_{IO}$[3] | −5 | - | +5 | µA |
| $I_{IL}$ | LOW-level input current | $V_{TXD}$ = 0 V | −260 | - | −30 | µA |
| $C_i$ | input capacitance | [4] | - | 5 | 10 | pF |
| **CAN receive data output; pin RXD** | | | | | | |
| $I_{OH}$ | HIGH-level output current | $V_{RXD} = V_{IO}$[3] − 0.4 V | −8 | −3 | −1 | mA |
| $I_{OL}$ | LOW-level output current | $V_{RXD}$ = 0.4 V; bus dominant | 1 | - | 12 | mA |
| **Bus lines; pins CANH and CANL** | | | | | | |
| $V_{O(dom)}$ | dominant output voltage | $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$ | | | | |
| | | pin CANH; $R_L$ = 50 Ω to 65 Ω | 2.75 | 3.5 | 4.5 | V |
| | | pin CANL; $R_L$ = 50 Ω to 65 Ω | 0.5 | 1.5 | 2.25 | V |
| $V_{dom(TX)sym}$ | transmitter dominant voltage symmetry | $V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$ | −400 | - | +400 | mV |
| $V_{TXsym}$ | transmitter voltage symmetry | $V_{TXsym} = V_{CANH} + V_{CANL}$; [4] [5]<br>$f_{TXD}$ = 250 kHz, 1 MHz and 2.5 MHz;<br>$C_{SPLIT}$ = 4.7 nF | $0.9V_{CC}$ | - | $1.1V_{CC}$ | V |
| $V_{O(dif)}$ | differential output voltage | dominant; $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$ | | | | |
| | | $R_L$ = 50 Ω to 65 Ω | 1.5 | - | 3 | V |
| | | $R_L$ = 45 Ω to 70 Ω | 1.4 | - | 3.3 | V |
| | | $R_L$ = 2240 Ω | 1.5 | - | 5 | V |
| | | recessive; $V_{TXD} = V_{IO}$[3]; no load | −50 | - | +50 | mV |
| $V_{O(rec)}$ | recessive output voltage | $V_{TXD} = V_{IO}$[3]; no load | 2 | $0.5V_{CC}$ | 3 | V |
| $V_{th(RX)dif}$ | differential receiver threshold voltage | Normal/Silent mode;<br>−12 V ≤ $V_{CANL}$ ≤ +12 V;<br>−12 V ≤ $V_{CANH}$ ≤ +12 V | 0.5 | - | 0.9 | V |
| $V_{rec(RX)}$ | receiver recessive voltage | −12 V ≤ $V_{CANL}$ ≤ +12 V;<br>−12 V ≤ $V_{CANH}$ ≤ +12 V | | | | |
| | | Normal/Silent mode | −4 | - | 0.5 | V |
| $V_{dom(RX)}$ | receiver dominant voltage | −12 V ≤ $V_{CANL}$ ≤ +12 V;<br>−12 V ≤ $V_{CANH}$ ≤ +12 V | | | | |
| | | Normal/Silent mode | 0.9 | - | 9.0 | V |
| $V_{hys(RX)dif}$ | differential receiver hysteresis voltage | Normal mode;<br>−12 V ≤ $V_{CANL}$ ≤ +12 V;<br>−12 V v $V_{CANH}$ ≤ +12 V | 50 | - | 300 | mV |
| $I_{O(sc)dom}$ | dominant short-circuit output current | $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$; $V_{CC}$ = 5 V | | | | |
| | | pin CANH; $V_{CANH}$ = −15 V to +40 V | −100 | −70 | −40 | mA |
| | | pin CANL; $V_{CANL}$ = −15 V to +40 V | 40 | 70 | 100 | mA |
| $I_{O(sc)rec}$ | recessive short-circuit output current | Normal mode; $V_{TXD} = V_{CC}$<br>$V_{CANH} = V_{CANL}$ = −27 V to +32 V | −5 | - | +5 | mA |

**Table 7. Static characteristics** *…continued*

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.75 V to 5.25 V; $V_{IO}$ = 2.95 V to 5.25 V[1]; $R_L$ = 60 Ω; $C_L$ = 100 pF unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC.[2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_L$ | leakage current | $V_{CC}$ = 0 V or $V_{CC}$ = $V_{IO}$ = shorted to ground via 47 kΩ; $V_{CANH}$ = $V_{CANL}$ = 5 V | −5 | - | +5 | µA |
| $R_i$ | input resistance | −2 V ≤ $V_{CANL}$ ≤ +7 V; −2 V ≤ $V_{CANH}$ ≤ +7 V [4] | 9 | 15 | 28 | kΩ |
| $\Delta R_i$ | input resistance deviation | 0 V ≤ $V_{CANL}$ ≤ +5 V; 0 V ≤ $V_{CANH}$ ≤ +5 V [4] | −3 | - | +3 | % |
| $R_{i(dif)}$ | differential input resistance | −2 V ≤ $V_{CANL}$ ≤ +7 V; −2 V ≤ $V_{CANH}$ ≤ +7 V [4] | 19 | 30 | 52 | kΩ |
| $C_{i(cm)}$ | common-mode input capacitance | [4] | - | - | 20 | pF |
| $C_{i(dif)}$ | differential input capacitance | [4] | - | - | 10 | pF |
| **Temperature detection** | | | | | | |
| $T_{j(sd)}$ | shutdown junction temperature | [4] | - | 185 | - | °C |

[1] Only TJA1057GT/3 and TJA1057GTK/3 have a $V_{IO}$ pin; the $V_{IO}$ input is internally connected to $V_{CC}$ in the other variants.

[2] Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[3] $V_{IO}$ = $V_{CC}$ in non-$V_{IO}$ product variants TJA1057(G)T(K).

[4] Not tested in production; guaranteed by design.

[5] The test circuit used to measure the bus output voltage symmetry (which includes $C_{SPLIT}$) is shown in Figure 8.

# 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.75 V to 5.25 V; $V_{IO}$ = 2.95 V to 5.25 V[1]; $R_L$ = 60 Ω; $C_L$ = 100 pF unless specified otherwise. All voltages are defined with respect to ground.[2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 7 and Figure 3** | | | | | | |
| $t_{d(TXD-busdom)}$ | delay time from TXD to bus dominant | Normal mode | - | 65 | - | ns |
| $t_{d(TXD-busrec)}$ | delay time from TXD to bus recessive | Normal mode | - | 90 | - | ns |
| $t_{d(busdom-RXD)}$ | delay time from bus dominant to RXD | Normal mode | - | 60 | - | ns |
| $t_{d(busrec-RXD)}$ | delay time from bus recessive to RXD | Normal mode | - | 65 | - | ns |
| $t_{d(TXDL-RXDL)}$ | delay time from TXD LOW to RXD LOW | TJA1057T; Normal mode | 50 | - | 230 | ns |
| | | TJA1057GT(/3), TJA1057GTK(/3); Normal mode | 50 | - | 210 | ns |
| $t_{d(TXDH-RXDH)}$ | delay time from TXD HIGH to RXD HIGH | TJA1057T; Normal mode | 50 | - | 230 | ns |
| | | TJA1057GT(/3), TJA1057GTK(/3); Normal mode | 50 | - | 210 | ns |
| $t_{bit(bus)}$ | transmitted recessive bit width | TJA1057GT(/3), TJA1057GTK(/3) | | | | |
| | | $t_{bit(TXD)}$ = 500 ns [3] | 435 | - | 530 | ns |
| | | $t_{bit(TXD)}$ = 200 ns [3] | 155 | - | 210 | ns |
| $t_{bit(RXD)}$ | bit time on pin RXD | TJA1057GT(/3), TJA1057GTK(/3) | | | | |
| | | $t_{bit(TXD)}$ = 500 ns [3] | 400 | - | 550 | ns |
| | | $t_{bit(TXD)}$ = 200 ns [3] | 120 | - | 220 | ns |
| $\Delta t_{rec}$ | receiver timing symmetry | TJA1057GT(/3), TJA1057GTK(/3) | | | | |
| | | $t_{bit(TXD)}$ = 500 ns | −65 | - | +40 | ns |
| | | $t_{bit(TXD)}$ = 200 ns | −45 | - | +15 | ns |
| $t_{to(dom)TXD}$ | TXD dominant time-out time | $V_{TXD}$ = 0 V; Normal mode | 0.8 | 3 | 6.5 | ms |

[1] Only TJA1057GT/3 and TJA1057GTK/3 have a $V_{IO}$ pin; the $V_{IO}$ input is internally connected to $V_{CC}$ in the other variants.

[2] Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[3] See Figure 4.

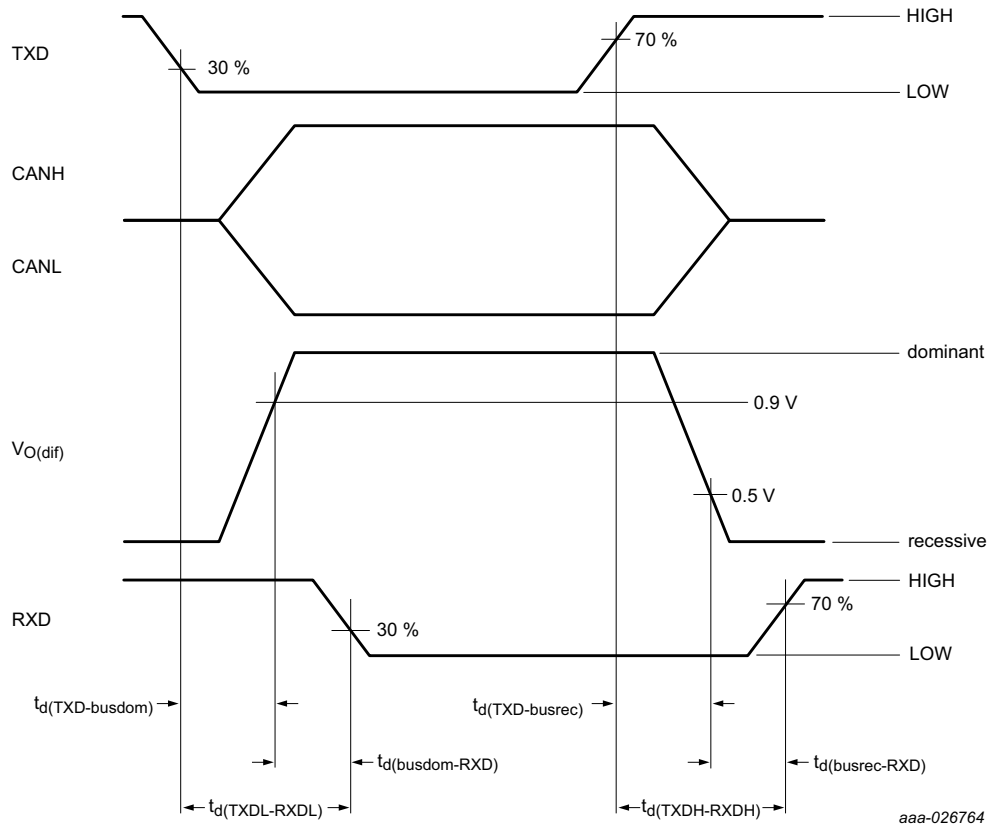



**Fig 3. CAN transceiver timing diagram**

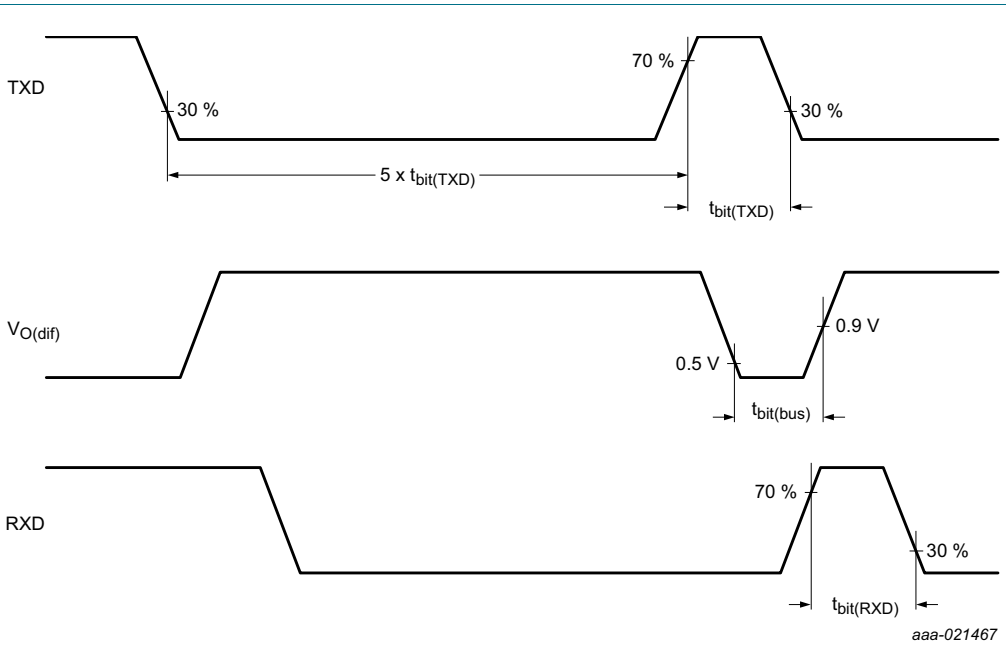
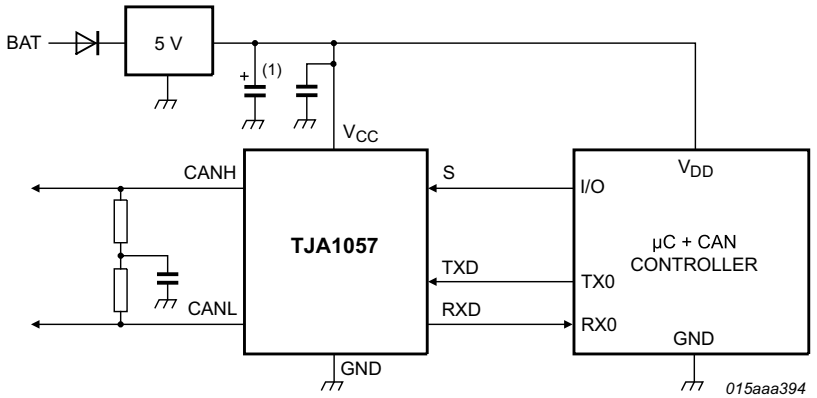



**Fig 4. CAN FD timing definitions according to ISO 11898-2:2016**

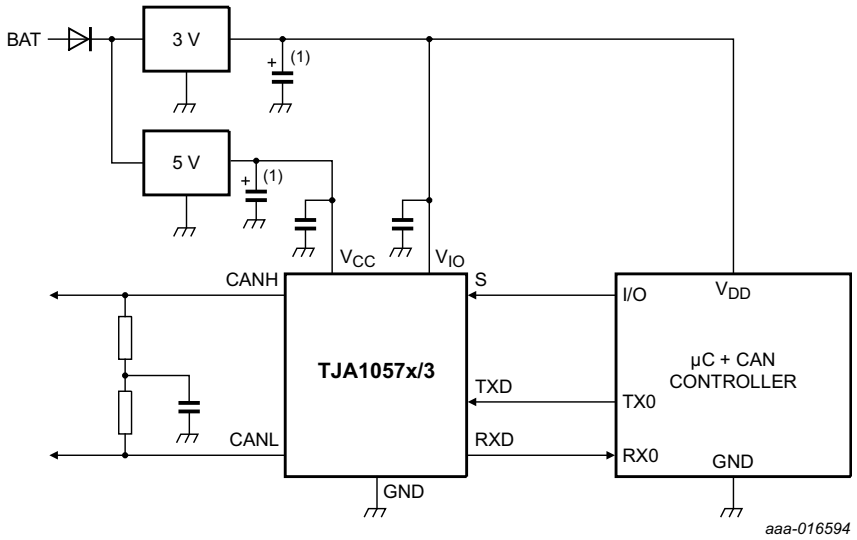
# 12. Application information

## 12.1 Application diagram




(1) Optional, depends on regulator.

**Fig 5. Typical TJA1057 application with a 5 V microcontroller (non-$V_{IO}$ variants)**



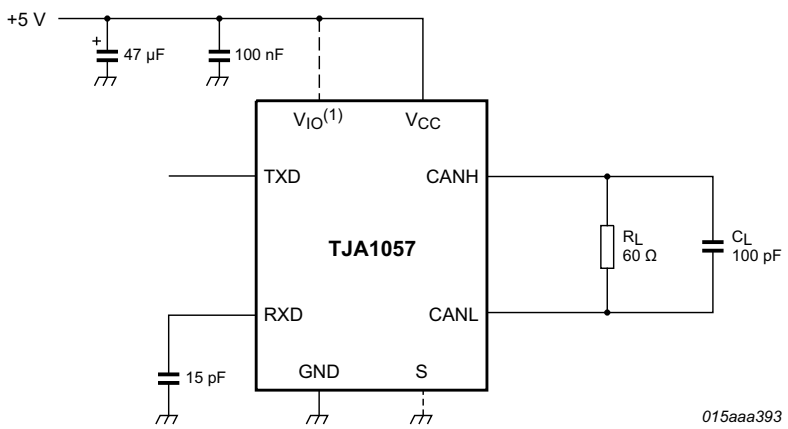

(1) Optional, depends on regulator.

**Fig 6. Typical application with a 3 V microcontroller for TJA1057x/3 $V_{IO}$ variants**

## 12.2 Application hints

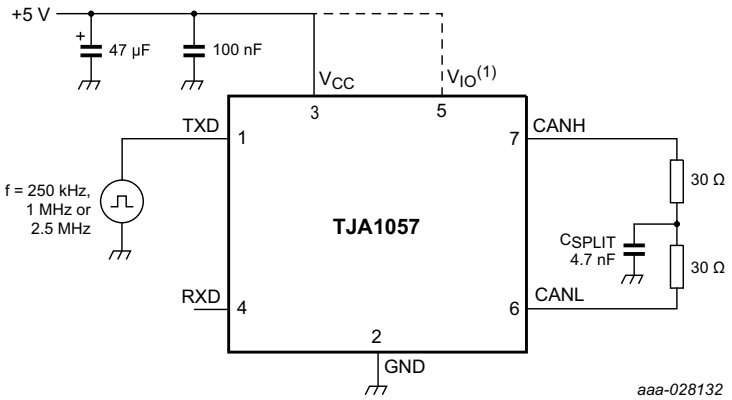
Further information on the application of the TJA1057 can be found in NXP application hints *AH1308 Application Hints - Standalone high-speed CAN transceivers Mantis TJA1044/TJA1057 and Dual-Mantis TJA1046*.

# 13. Test information




(1) The $V_{IO}$ pin is internally connected to pin $V_{CC}$ in the non-$V_{IO}$ product variants TJA1057(G)T(K).

**Fig 7. CAN transceiver timing test circuit**




(1) The $V_{IO}$ pin is internally connected to pin $V_{CC}$ in the non-$V_{IO}$ product variants TJA1057(G)T(K).

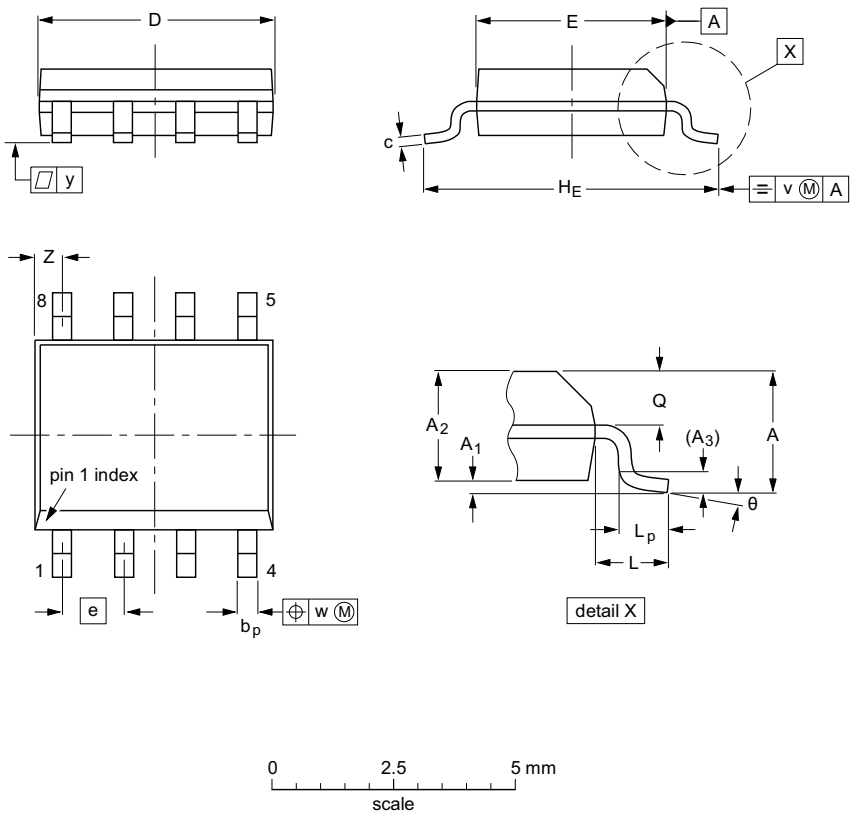
**Fig 8. Test circuit for measuring transceiver driver symmetry**

## 13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

# 14. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

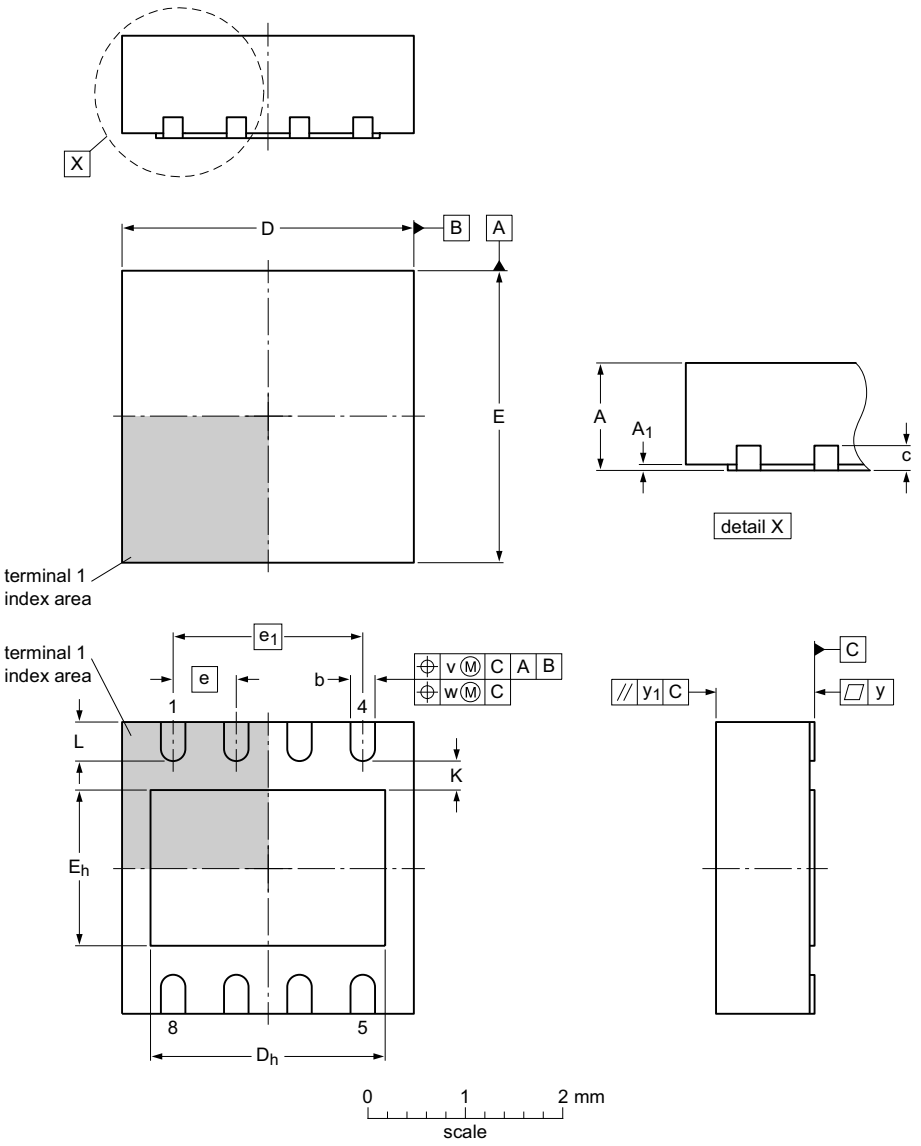
**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 9. Package outline SOT96-1 (SO8)**

**HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm** **SOT782-1**




Dimensions

| Unit(1) | | A | $A_1$ | b | c | D | $D_h$ | E | $E_h$ | e | $e_1$ | K | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.35 | | 3.10 | 2.45 | 3.10 | 1.65 | | | 0.35 | 0.45 | | | | |
| mm | nom | 0.85 | 0.03 | 0.30 | 0.2 | 3.00 | 2.40 | 3.00 | 1.60 | 0.65 | 1.95 | 0.30 | 0.40 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.25 | | 2.90 | 2.35 | 2.90 | 1.55 | | | 0.25 | 0.35 | | | | |

Note

1. Plastic or metal protrusions of 0.075 maximum per side are not included.

*sot782-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT782-1 | - - - | MO-229 | - - - | | | ~~09-08-25~~ 09-08-28 |

**Fig 10. Package outline SOT782-1 (HVSON8)**

# 15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

# 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

**Table 9. SnPb eutectic process (from J-STD-020D)**

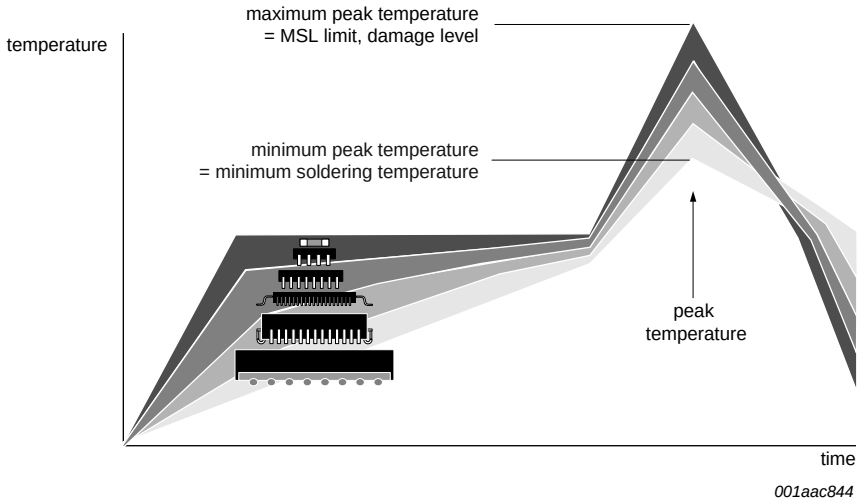
| **Package thickness (mm)** | **Package reflow temperature (°C)** | |
|---|---|---|
| | **Volume ($mm^3$)** | |
| | **< 350** | **≥ 350** |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 10. Lead-free process (from J-STD-020D)**

| **Package thickness (mm)** | **Package reflow temperature (°C)** | | |
|---|---|---|---|
| | **Volume ($mm^3$)** | | |
| | **< 350** | **350 to 2000** | **> 2000** |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.




MSL: Moisture Sensitivity Level

**Fig 11. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

# 17. Appendix: ISO 11898-2:2016 parameter cross-reference list

**Table 11. ISO 11898-2:2016 to NXP data sheet parameter conversion**

| ISO 11898-2:2016 | | NXP data sheet | |
|---|---|---|---|
| **Parameter** | **Notation** | **Symbol** | **Parameter** |
| **HS-PMA dominant output characteristics** | | | |
| Single ended voltage on CAN_H | $V_{CAN\_H}$ | $V_{O(dom)}$ | dominant output voltage |
| Single ended voltage on CAN_L | $V_{CAN\_L}$ | | |
| Differential voltage on normal bus load | $V_{Diff}$ | $V_{O(dif)}$ | differential output voltage |
| Differential voltage on effective resistance during arbitration | | | |
| Optional: Differential voltage on extended bus load range | | | |
| **HS-PMA driver symmetry** | | | |
| Driver symmetry | $V_{SYM}$ | $V_{TXsym}$ | transmitter voltage symmetry |
| **Maximum HS-PMA driver output current** | | | |
| Absolute current on CAN_H | $I_{CAN\_H}$ | $I_{O(sc)dom}$ | dominant short-circuit output current |
| Absolute current on CAN_L | $I_{CAN\_L}$ | | |
| **HS-PMA recessive output characteristics, bus biasing active/inactive** | | | |
| Single ended output voltage on CAN_H | $V_{CAN\_H}$ | $V_{O(rec)}$ | recessive output voltage |
| Single ended output voltage on CAN_L | $V_{CAN\_L}$ | | |
| Differential output voltage | $V_{Diff}$ | $V_{O(dif)}$ | differential output voltage |
| **Optional HS-PMA transmit dominant timeout** | | | |
| Transmit dominant timeout, long | $t_{dom}$ | $t_{to(dom)TXD}$ | TXD dominant time-out time |
| Transmit dominant timeout, short | | | |
| **HS-PMA static receiver input characteristics, bus biasing active/inactive** | | | |
| Recessive state differential input voltage range<br>Dominant state differential input voltage range | $V_{Diff}$ | $V_{th(RX)dif}$ | differential receiver threshold voltage |
| | | $V_{rec(RX)}$ | receiver recessive voltage |
| | | $V_{dom(RX)}$ | receiver dominant voltage |
| **HS-PMA receiver input resistance (matching)** | | | |
| Differential internal resistance | $R_{Diff}$ | $R_{i(dif)}$ | differential input resistance |
| Single ended internal resistance | $R_{CAN\_H}$<br>$R_{CAN\_L}$ | $R_i$ | input resistance |
| Matching of internal resistance | MR | $\Delta R_i$ | input resistance deviation |
| **HS-PMA implementation loop delay requirement** | | | |
| Loop delay | $t_{Loop}$ | $t_{d(TXDH-RXDH)}$ | delay time from TXD HIGH to RXD HIGH |
| | | $t_{d(TXDL-RXDL)}$ | delay time from TXD LOW to RXD LOW |
| **Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s** | | | |
| Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended | $t_{Bit(Bus)}$ | $t_{bit(bus)}$ | transmitted recessive bit width |
| Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s | $t_{Bit(RXD)}$ | $t_{bit(RXD)}$ | bit time on pin RXD |
| Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s | $\Delta t_{Rec}$ | $\Delta t_{rec}$ | receiver timing symmetry |

**Table 11. ISO 11898-2:2016 to NXP data sheet parameter conversion**

| ISO 11898-2:2016 | | NXP data sheet | |
|---|---|---|---|
| **Parameter** | **Notation** | **Symbol** | **Parameter** |
| **HS-PMA maximum ratings of $V_{CAN\_H}$, $V_{CAN\_L}$ and $V_{Diff}$** | | | |
| Maximum rating $V_{Diff}$ | $V_{Diff}$ | $V_{(CANH-CANL)}$ | voltage between pin CANH and pin CANL |
| General maximum rating $V_{CAN\_H}$ and $V_{CAN\_L}$ | $V_{CAN\_H}$ $V_{CAN\_L}$ | $V_x$ | voltage on pin x |
| Optional: Extended maximum rating VCAN_H and VCAN_L | | | |
| **HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered** | | | |
| Leakage current on CAN_H, CAN_L | $I_{CAN\_H}$ $I_{CAN\_L}$ | $I_L$ | leakage current |
| **HS-PMA bus biasing control timings** | | | |
| CAN activity filter time, long | $t_{Filter}$ | $t_{wake(busdom)}$[1] | bus dominant wake-up time |
| CAN activity filter time, short | | $t_{wake(busrec)}$[1] | bus recessive wake-up time |
| Wake-up timeout, short | $t_{Wake}$ | $t_{to(wake)bus}$ | bus wake-up time-out time |
| Wake-up timeout, long | | | |
| Timeout for bus inactivity | $t_{Silence}$ | $t_{to(silence)}$ | bus silence time-out time |
| Bus Bias reaction time | $t_{Bias}$ | $t_{d(busact-bias)}$ | delay time from bus active to bias |

[1] $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

## 18. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TJA1057 v.6 | 20170824 | Product data sheet | - | TJA1057 v.5.1 |
| Modifications: | • Updated to comply with ISO 11898-2:2016 and SAE J22884-1 through SAE J2284-5 specifications:<br>– Table 7: conditions added to parameters $R_i$, $\Delta R_i$ and $R_{i(dif)}$; values/conditions changed for parameters $I_{CC}$, $V_{rec(RX)}$, $V_{dom(RX)}$, $I_{O(sc)dom}$<br>– Additional measurement taken at $f_{TXD}$ = 1 MHz and 2.5 MHz for parameter $V_{TXsym}$; see Table 7 "Static characteristics" and Figure 8<br>– Thresholds clarified in Figure 3<br>• Section 2.1: text of last entry amended<br>• Table 2: Table note 1 amended<br>• Table 5, Table note 2 added<br>• Amended Figure 3, Figure 5, Figure 6 and Figure 8; figure title changed on Figure 4<br>• Section 12.2: reference updated | | | |
| TJA1057 v.5.1 | 20160523 | Product data sheet | - | TJA1057 v.5 |
| TJA1057 v.5 | 20160128 | Product data sheet | - | TJA1057 v.4 |
| TJA1057 v.4 | 20150710 | Product data sheet | - | TJA1057 v.3 |
| TJA1057 v.3 | 20141119 | Product data sheet | - | TJA1057 v.2 |
| TJA1057 v.2 | 20131030 | Product data sheet | - | TJA1057 v.1 |
| TJA1057 v.1 | 20130530 | Preliminary data sheet | - | - |

# 19. Legal information

## 19.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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# 21. Contents





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**Document identifier: TJA1057**