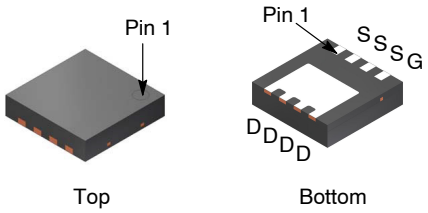
MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

100 V, 43 A, 14 mΩ

FDMC86160

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
100 V	14 mΩ @ 10 V	43 A
	23 mΩ @ 6 V	



Top Bottom

WDFN8 3.3X3.3, 0.65P
CASE 483AW

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced PowerTrench process that incorporates Shielded Gate technology. This process has been optimized for the on−state resistance. This device is well suited for applications where ulta low $R_{DS(on)}$ is required in small spaces such as High performance VRM, POL and orring functions.

Applications

- Bridge Topologies
- Synchronous Rectifier

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 14 mΩ at V_{GS} = 10 V, I_D = 9 A
- Max $r_{DS(on)}$ = 23 mΩ at V_{GS} = 6 V, I_D = 7 A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- This Device is Lead−Free and RoHS Compliant

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DSS}	Drain−Source Voltage	100	V
V_{GSS}	Gate−Source Voltage	±20	V
I_D	Drain Current − Continuous (T_C = 25°C) − Continuous (T_A = 25°C) (Note 1a) − Pulsed (Note 4)	 43 9 50	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	181	mJ
P_D	Power Dissipation (T_C = 25°C) (T_A = 25°C) (Note 1a)	 54 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

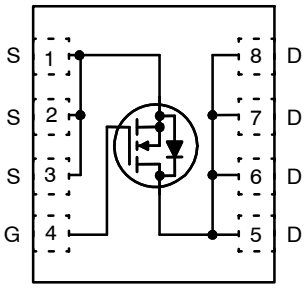
THERMAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Ambient (Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Case (Note 1a)	53	°C/W

MARKING DIAGRAM

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDMC86160	WDFN8 3.3X3.3, 0.65P CASE 483AW (Pb−Free)	3000 / Tape & Reel

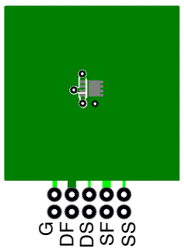
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

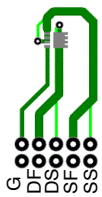
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	73	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–9	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 9 A	–	11.2	14	mΩ
		V_{GS} = 6 V, I_D = 7 A	–	16	23	
		V_{GS} = 10 V, I_D = 9 A, T_J = 125°C	–	21	26	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 9 A	–	43	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	968	1290	pF
C_{oss}	Output Capacitance		–	241	320	pF
C_{rss}	Reverse Transfer Capacitance		–	11	20	pF
R_g	Gate Resistance		0.1	0.6	2.5	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 50 V, I_D = 9 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	9.7	19	ns
t_r	Rise Time		–	3.6	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	16	30	ns
t_f	Fall Time		–	3.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 9 A	–	15	22	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 6 V; V_{DD} = 50 V, I_D = 9 A	–	9.8	15	nC
Q_{gs}	Total Gate Charge	V_{DD} = 50 V, I_D = 9 A	–	4.4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 9 A	–	3.5	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 9 A (Note 2)	–	0.79	1.3	V
		V_{GS} = 0 V, I_S = 1.9 A (Note 2)	–	0.72	1.2	
t_{rr}	Reverse Recovery Time	I_F = 9 A, di/dt = 100 A/μs	–	47	75	ns
Q_{rr}	Reverse Recovery Charge		–	45	73	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR–4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined bythe user’s board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 181 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 11 A, V_{DD} = 100 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 35 A.
4. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

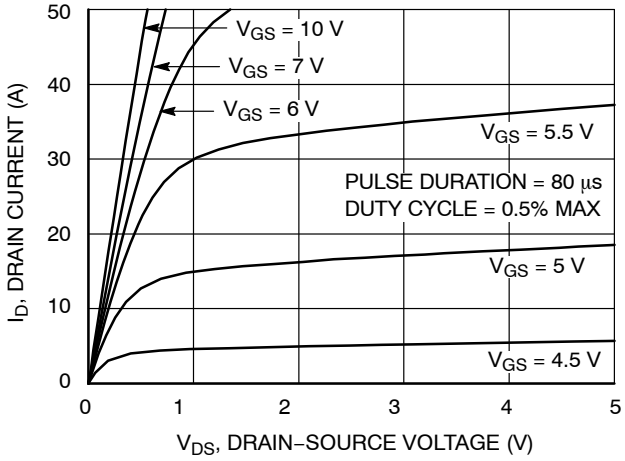


Figure 1. On−Region Characteristics

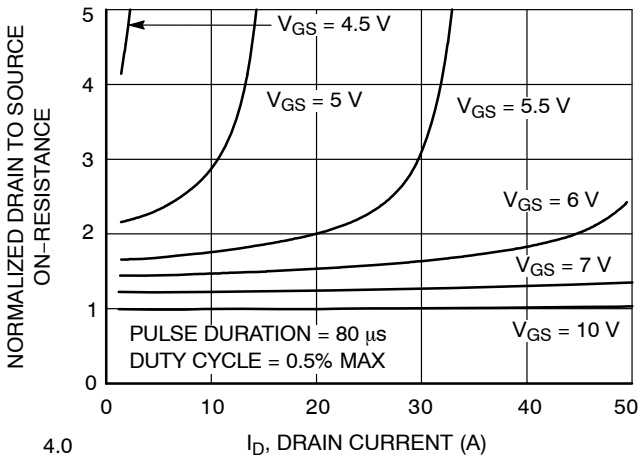


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

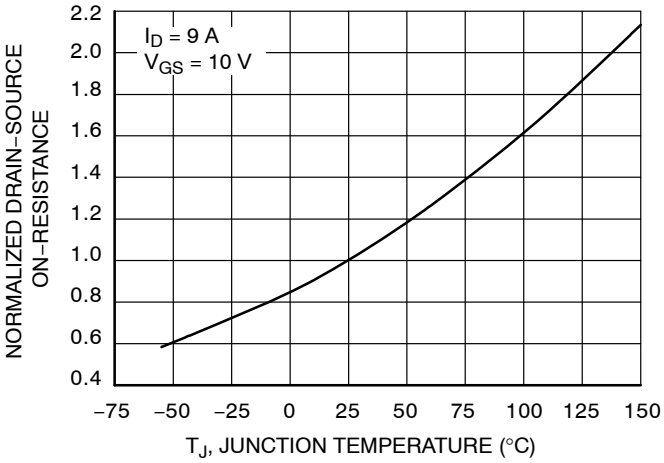


Figure 3. Normalized On−Resistance vs Junction Temperature

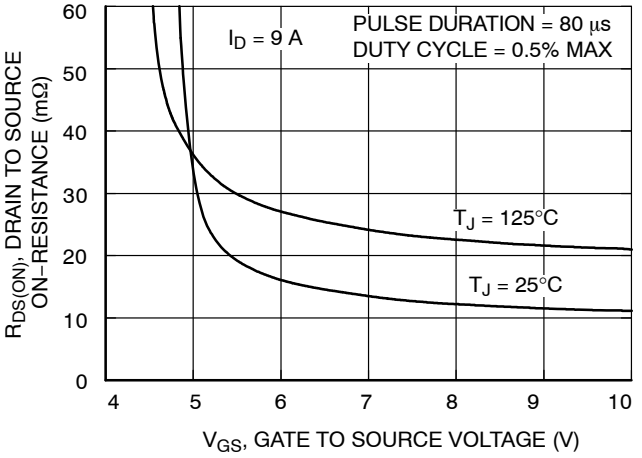


Figure 4. On−Resistance vs Gate to Source Voltage

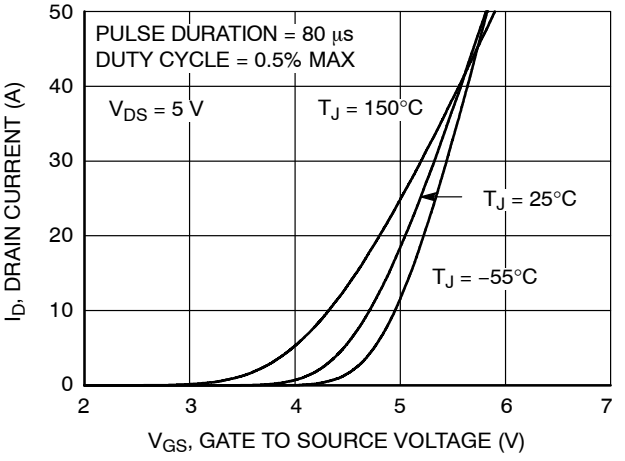


Figure 5. Transfer Characteristics

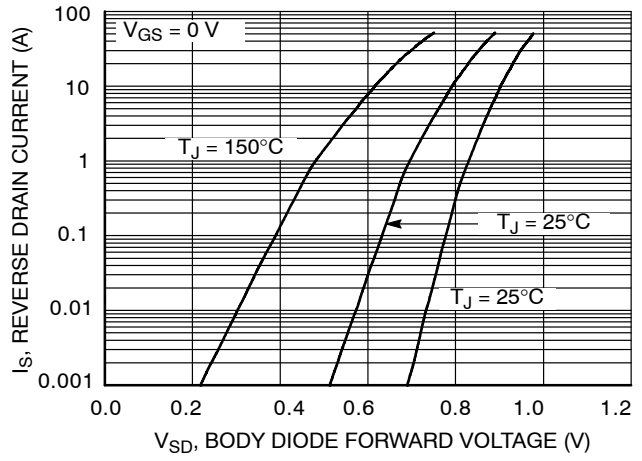


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

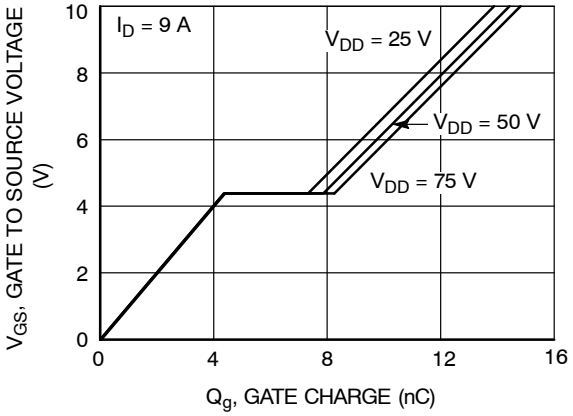


Figure 7. Gate Charge Characteristics

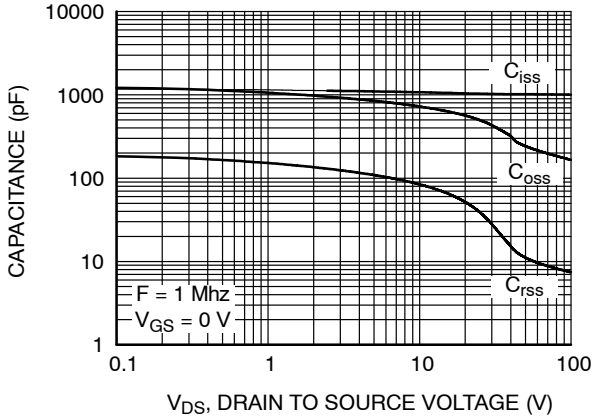


Figure 8. Capacitance vs Drain to Source Voltage

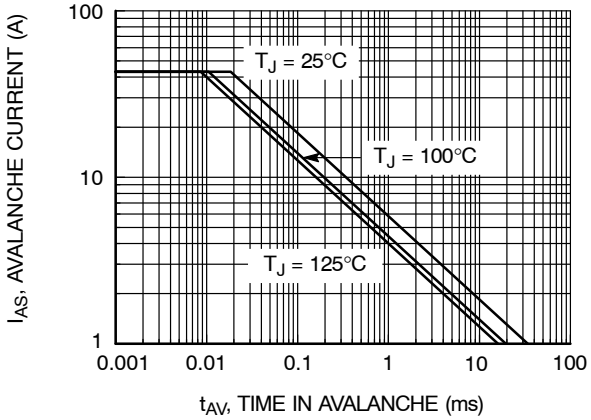


Figure 9. Unclamped Inductive Switching Capability

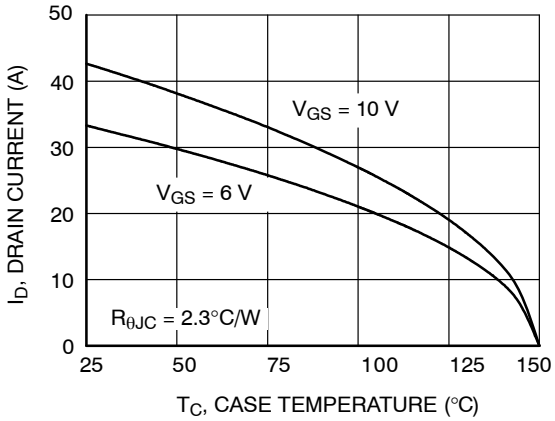


Figure 10. Maximum Continuous Drain Current vs Case Temperature

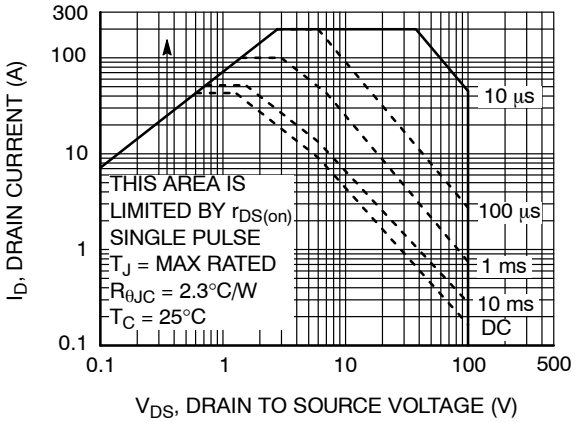


Figure 11. Forward Bias Safe Operating Area

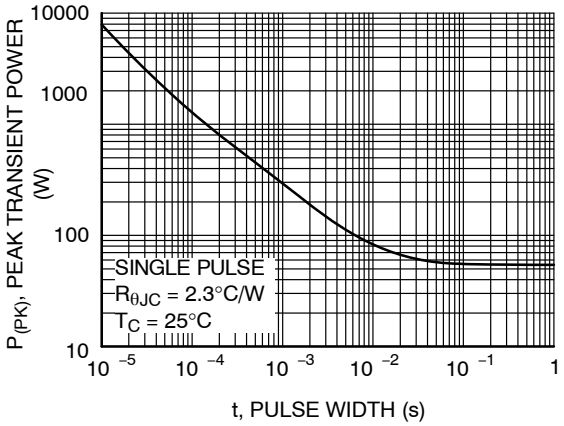


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

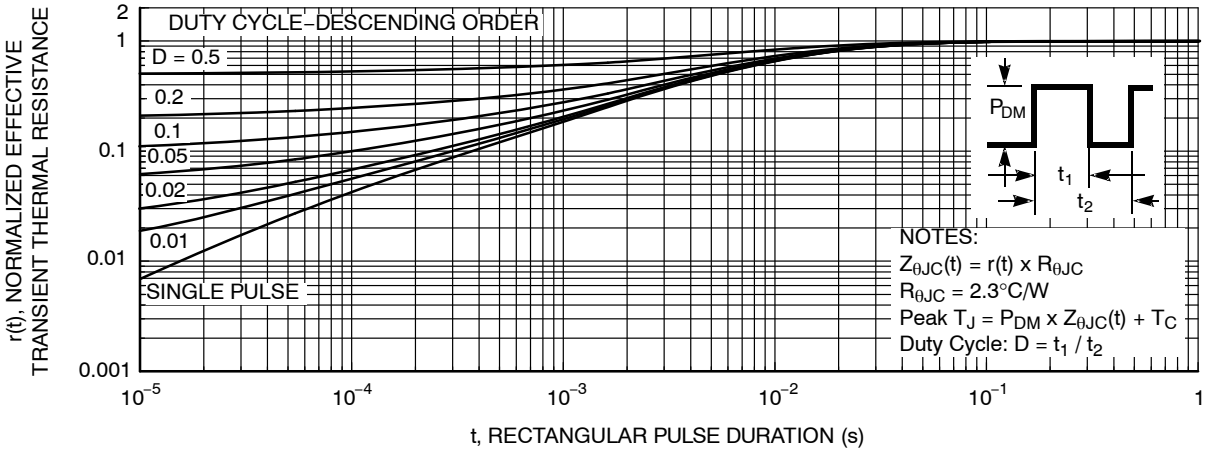
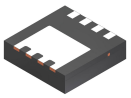


Figure 13. Junction−to−Case Transient Thermal Response Curve

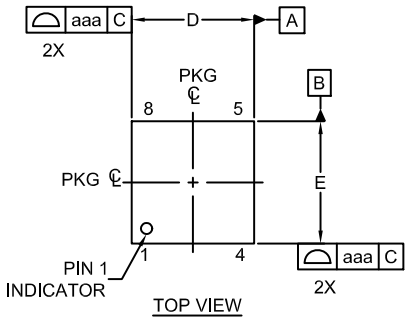
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

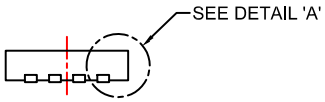


WDFN8 3.3X3.3, 0.65P
CASE 483AW
ISSUE A

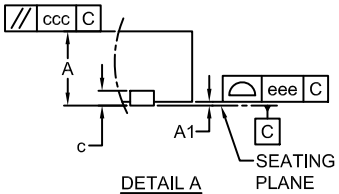
DATE 10 SEP 2019



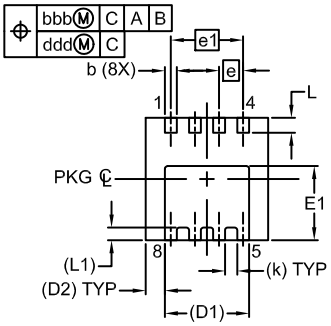
TOP VIEW



FRONT VIEW

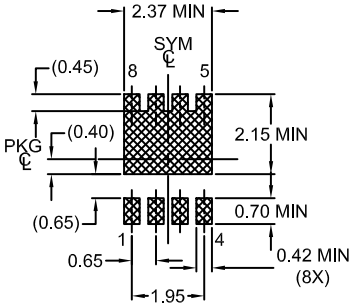


DETAIL A
SCALE: 2x



BOTTOM VIEW

LAND PATTERN RECOMMENDATION*



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

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