Product Change Notification / SYST-01SBDY255

Date:

08-Dec-2020

Product Category:

USB Security Controllers

PCN Type:

Document Change

Notification Subject:

Data Sheet - SEC1110/SEC1210 - Smart Card Bridge to USB and UART Interfaces Data Sheet Data Sheet Document Revision

Affected CPNs:

SYST-01SBDY255_Affected_CPN_12082020.pdf
SYST-01SBDY255_Affected_CPN_12082020.csv

Notification Text:

SYST-01SBDY255

Microchip has released a new Product Documents for the SEC1110/SEC1210 - Smart Card Bridge to USB and UART Interfaces Data Sheet of devices. If you are using one of these devices please read the document located at SEC1110/SEC1210 - Smart Card Bridge to USB and UART Interfaces Data Sheet.

Notification Status: Final

Description of Change: This revision includes the following changes

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION

DS00001561D (11-17-20)	All	Master/Slave terms are deprecated and replacedby more accurate terms depending on the context nevertheless theseterms might be still used in the specifications listed in Appendix B: "References". Register and bit names remain unchanged, only their descriptions change.
	Cover sheet, Section 1.1 on page 4	Feature Highlights: SPI • Master capability with 12 MHz max performance -> Host capability with 12 MHz max performance
	Table 5-1 on page 13	SPI1 Chip Enable: Master mode -> Host mode
		SPI1 Clock: Master mode -> Host mode
		SPI1 Data In: Master data -> Host data
		SPI1 Data Out: Master data -> Host data
	FIGURE 7-1: on page 20	SPI Master -> SPI Host
	Table 7-3 on page 22	2x: SPI2 CODE MASTER -> SPI2 CODE MAIN
	Table 9-34 on page 42	Bit 5: Synchronous Serial Slave -> Synchronous Serial Client Bit 4: configured as Master -> configured asHost, selected as Slave -> selected as Client
	Section 9.1.24 on page 42	(Slave select) -> (Client select)
	Section 9.1.25 on page 43	Master clock rate -> Host clock rate
	Table 9-35 on page 43	Bit 7: Master Mode -> Host Mode
		Bit 4: Serial Peripheral Master -> Serial Peripheral Host, SPI1 as a Master -> SPI1 as a Host
		Bit 1:0: Master Mode -> Host Mode
	Table 9-36 on page 44	The Master clock -> The Host clock
	FIGURE 10-3: on page 47	XDATA SLAVE -> XDATA
	Table 10-4 on page 67	Offset address: 0x0006: Block Master Control -> Block Main Control
	Table 10-20 on page 78	Title and caption: Block Master -> Block Main
		Bit 0: Software-Controlled Master -> Software-Controlled Main
	Note 12-1	The SPI2 Master -> The SPI2 Host

	Section 14.0 on page 145	Title: Master ->Host... works as a Master device -> ... works as a Host device Master Mode -> Host Mode Master baud rates ->Host baud rates Slave Select Output -> Client Select Output slave devices -> client devices Master functionality -> Host functionality Master clock -> Host clock
	FIGURE 14-1: on page 146	Title: SPI1 Master -> SPI1 Host
	Section 14.1 on page 146	Title: Master-> Host Master Mode -> Host Mode from the Slave -> from the Client Master clock ->Host clock Master or Slave -> Host or Client Slave on Master's misoi -> Client on Host's misoi
	FIGURE 14-2: on page 147	Title: Master-> Host Master -> Host
	FIGURE 14-3: on page 148	Title: MasterMode -> Host Mode Master -> Host
	FIGURE 14-4: on page 148	Title: MasterMode -> Host Mode Master -> Host
	FIGURE 14-5: on page 149	Title: MasterMode -> Host Mode Master -> Host
	Section 15.4.9 on page 158	Master SPI interface -> Host SPI interface
	Section 15.4.10 on page 158	Master SPI interface -> Host SPI interface
	Table 16-3 on page 178	Bit 3: Byte Enable MasterFuse -> Byte Enable Main Fuse
	Table 18-4, "Package Thermal Resistance Parameters," on page 195	Package Thermal Specifications adopted

Impacts to Data Sheet: None
Reason for Change: To Improve Manufacturability
Change Implementation Status: Complete

Date Document Changes Effective: 08 December 2020
NOTE: Please be advised that this is a change to the document only the product has not been changed.
Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SEC1110/SEC1210 - Smart Card Bridge to USB and UART Interfaces Data Sheet

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Affected Catalog Part Numbers (CPN)

SEC1110-1100A5
SEC1110-A5-02
SEC1110-A5-02-TR
SEC1110-A5-02G1
SEC1110-A5-02NC
SEC1110-A5-02NC-TR
SEC1110-A5-03G1
SEC1110-A5-04G1
SEC1110I-A5-02
SEC1110I-A5-02-TR
SEC1110I-A5-02G1
SEC1210-A5-02G1
SEC1210-A5-02G1-TR
SEC1210-CN-02
SEC1210-CN-02-TR
SEC1210-CN-02NC
SEC1210-CN-02NC-TR
SEC1210-I/PV-UR2
SEC1210-I/PV-URT
SEC1210/PV-UR2
SEC1210/PV-URT
SEC1210I-A5-02G1
SEC1210I-A5-02G1-TR
SEC1210I-CN-02
SEC1210I-CN-02-TR
SEC1210T-I/PV-UR2
SEC1210T-I/PV-URT
SEC1210T/PV-UR2
SEC1210T/PV-URT