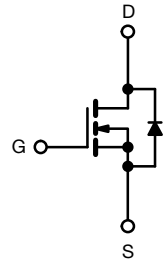


Power MOSFET



N-Channel MOSFET

FEATURES

- For automatic insertion
- Compact plastic package
- End stackable
- Fast switching
- Low drive current
- Easily paralleled
- Excellent temperature stability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRODUCT SUMMARY

V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.8
Q_g (Max.) (nC)	7	
Q_{gs} (nC)	2	
Q_{gd} (nC)	7	
Configuration	Single	

DESCRIPTION

The HVMDIP technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HVMDIP design achieves very low on-state resistance combined with high transconductance and extreme device ruggedness. HVMDIPs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HVMDIP 4 pin, dual-in-line package brings the advantages of HVMDIPs to high volume applications where automatic PC board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment, and consumer products. Their compatibility with automatic insertion equipment, low-profile and end stackable features represent the state-of-the-art in power device packaging.

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD113PbF

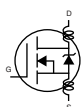
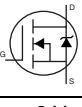
ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source Voltage ^a	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	I_D	0.8	A
Pulsed drain current ^b	I_{DM}	6.4	
Linear derating factor		0.008	W/ $^\circ\text{C}$
Inductive current, clamped	I_{LM}	6.4	A
Maximum power dissipation	P_D	1.0	W
Operating junction and storage temperature range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering recommendations (peak temperature)	for 10 s	300 $^\circ\text{C}$	

Notes

- $T_J = 25\text{ }^\circ\text{C}$ to 150 $^\circ\text{C}$
- Repetitive rating; pulse width limited by maximum junction temperature
- 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{max. rating}, V_{GS} = 0\text{ V}$		-	-	250	μA
		$V_{DS} = \text{max. rating} \times 0.8, V_{GS} = 0\text{ V}, T_C = 125\text{ }^\circ\text{C}$		-	-	1000	
On-State Drain Current ^b	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max.	0.8	-	-	A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 0.8\text{ A}$	-	0.6	0.8	Ω
Forward Transconductance ^b	g_{fs}	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., $I_D = 0.8\text{ A}$		0.8	1.2	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$		-	135	200	pF
Output Capacitance	C_{oss}			-	80	100	
Reverse Transfer Capacitance	C_{rss}			-	20	25	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 4\text{ A}, V_{DS} = 0.8\text{ max. rating}$	-	5	7	nC
Gate-Source Charge	Q_{gs}			-	2	-	
Gate-Drain Charge	Q_{gd}			-	7	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 0.5 V_{DS}, I_D = 0.8\text{ A}, R_g = 50\text{ }\Omega$		-	10	20	ns
Rise Time	t_r			-	15	25	
Turn-Off Delay Time	$t_{d(off)}$			-	15	25	
Fall Time	t_f			-	10	20	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	0.8	A
Pulsed Diode Forward Current	I_{SM}			-	-	6.4	
Body Diode Voltage ^a	V_{SD}	$T_A = 25\text{ }^\circ\text{C}, I_S = 0.8\text{ A}, V_{GS} = 0\text{ V}$		-	-	2	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 150\text{ }^\circ\text{C}, I_F = 1.0\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		-	100	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.2	-	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

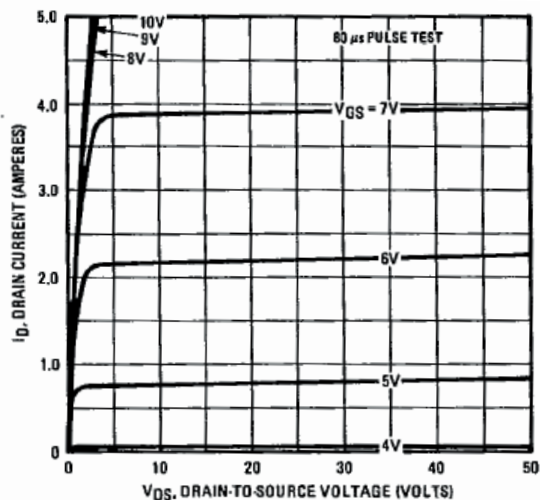


Fig. 1 - Typical Output Characteristics

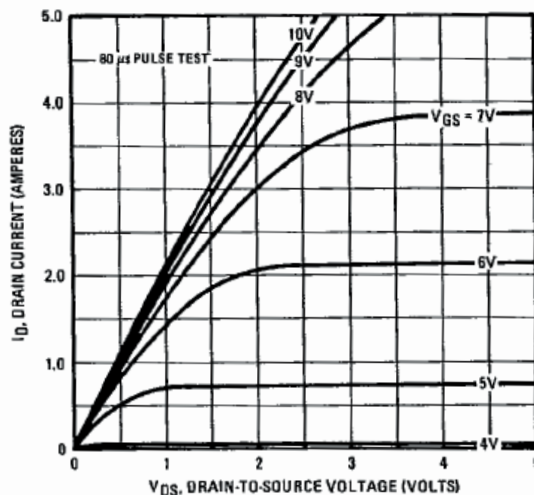


Fig. 2 - Typical Saturation Characteristics

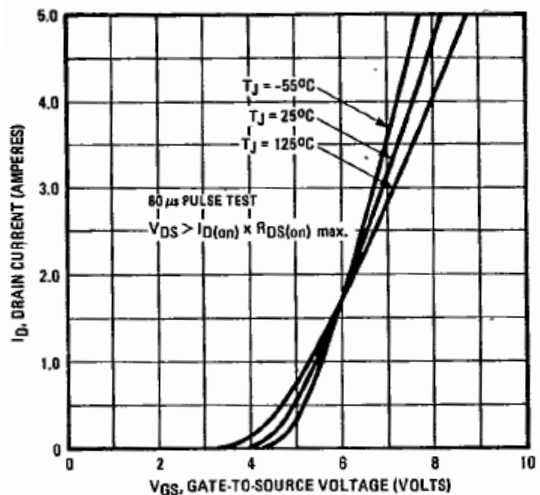


Fig. 1 - Typical Transfer Characteristics

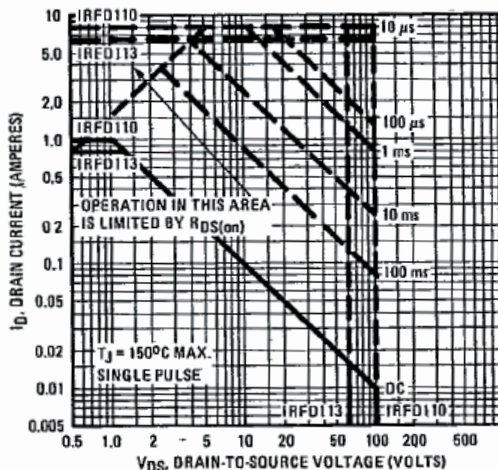


Fig. 3 - Maximum Safe Operating Area

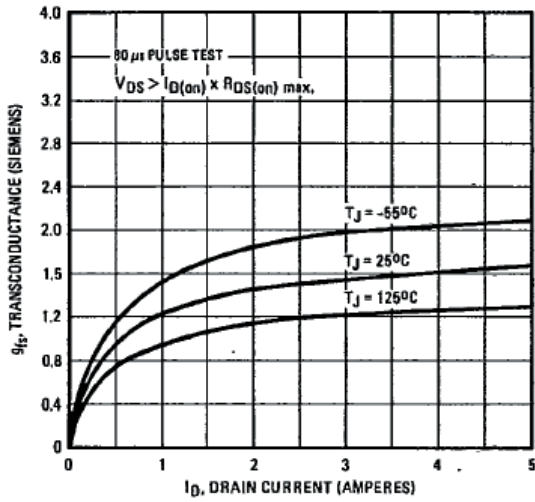


Fig. 4 - Typical Transconductance vs. Drain Current

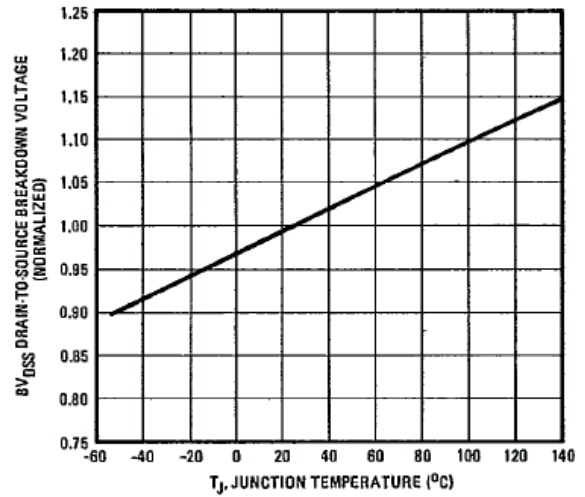


Fig. 6 - Breakdown Voltage vs. Temperature

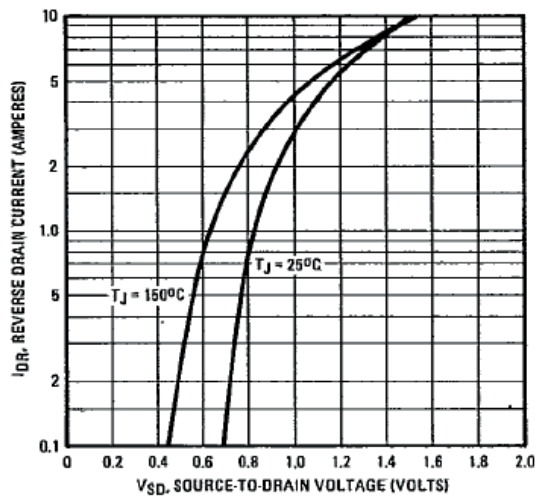


Fig. 5 - Typical Source-Drain Diode Forward Voltage

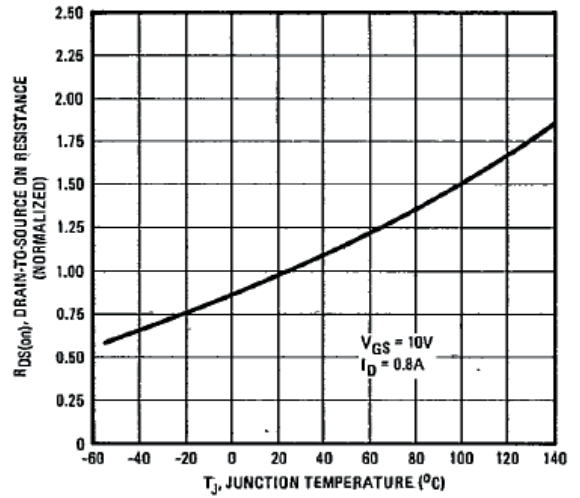


Fig. 7 - Normalized On-Resistance vs. Temperature

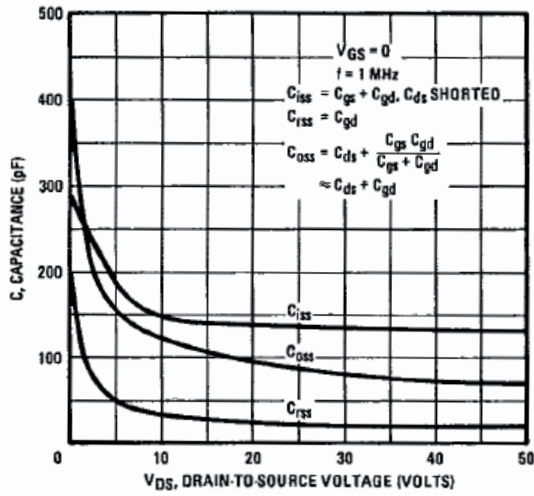


Fig. 8 - Typical Capacitance vs. Drain-to-Source Voltage

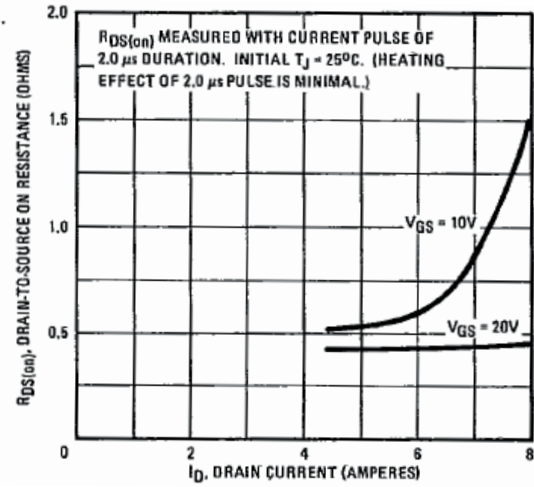


Fig. 10 - Typical On-Resistance vs. Darin Current

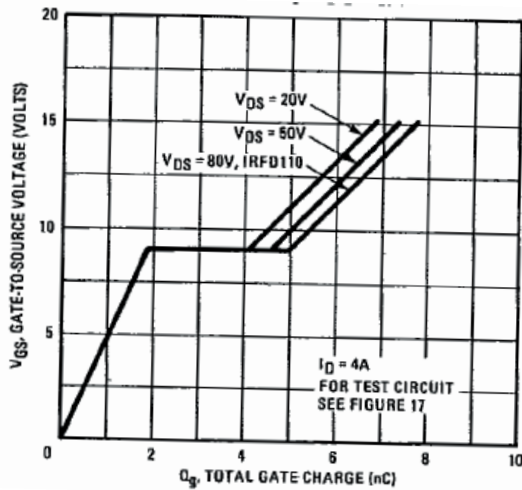


Fig. 9 - Typical Gate Charge vs. Gate-to-Source Voltage

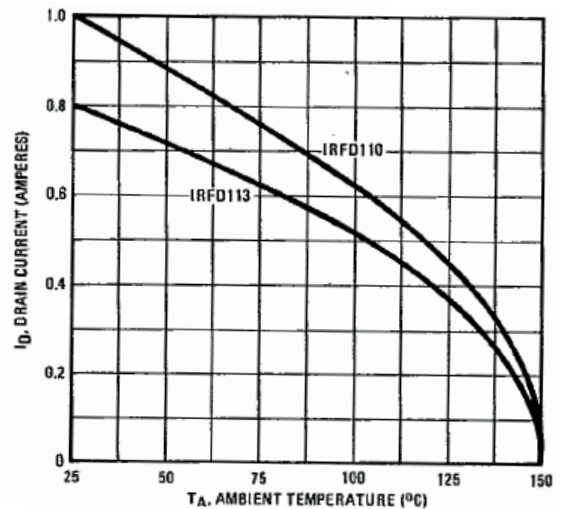


Fig. 11 - Maximum Darin Current vs. Case Temperature

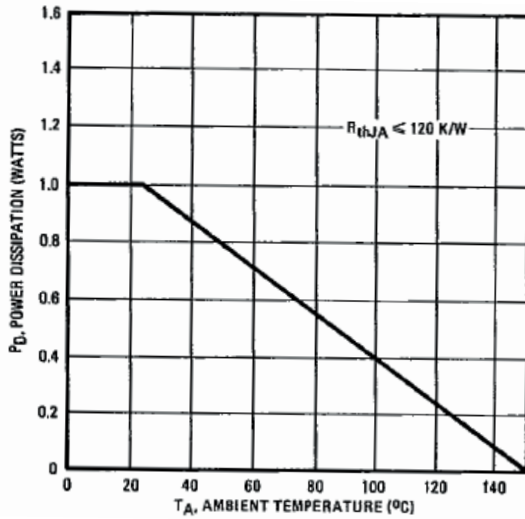


Fig. 12 - Power vs. Temperature Derating

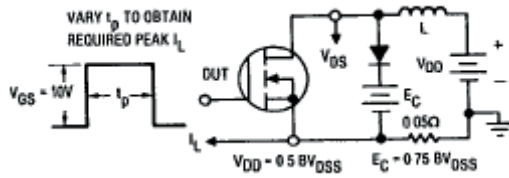


Fig. 13 - Clamped Inductive Test Circuit

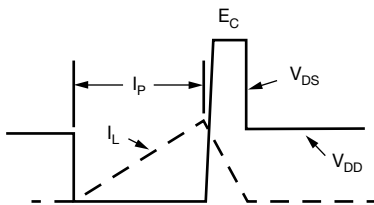


Fig. 14 - Clamped Inductive Waveforms

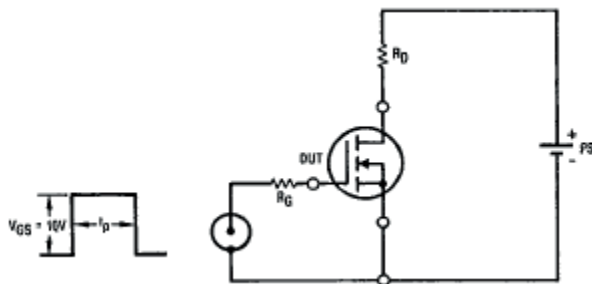


Fig. 15 - Switching Time Test Circuit

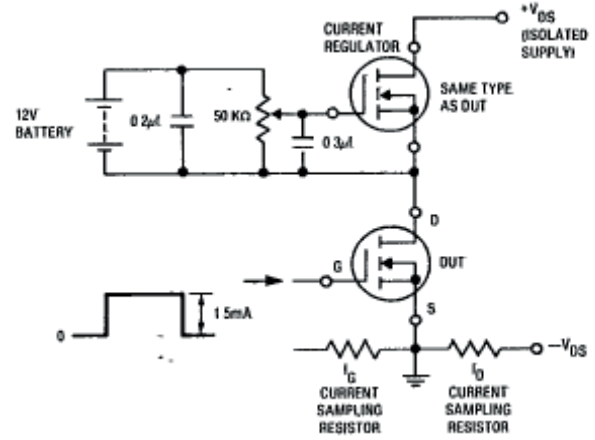


Fig. 16 - Gate Charge Test Circuit

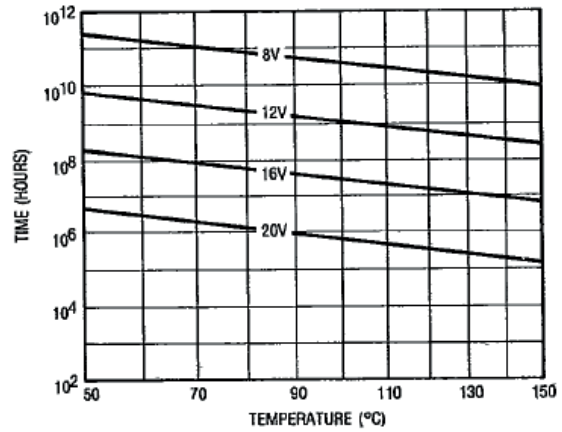


Fig. 17 - Typical Time to Accumulated 1% Gate Failure

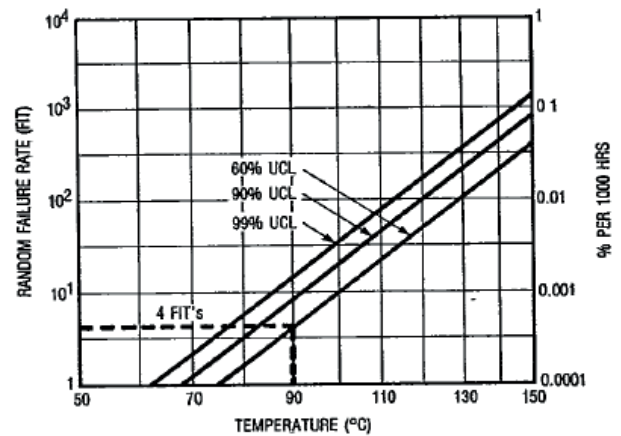
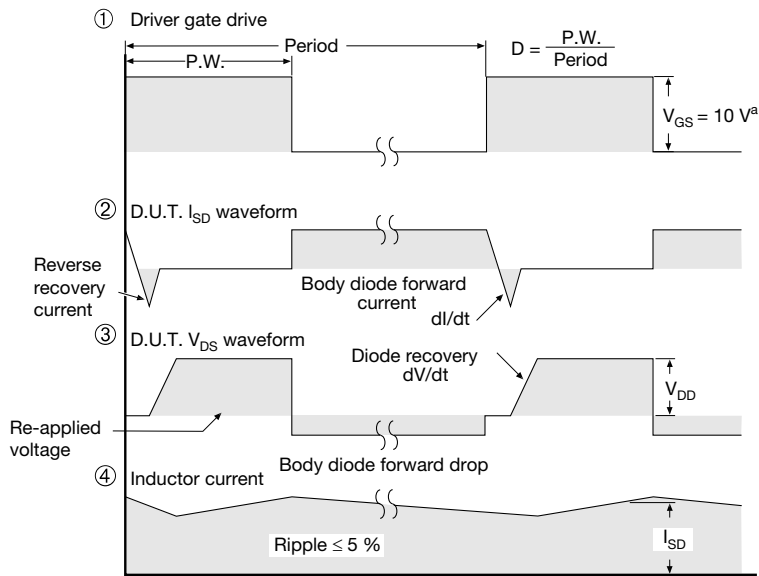
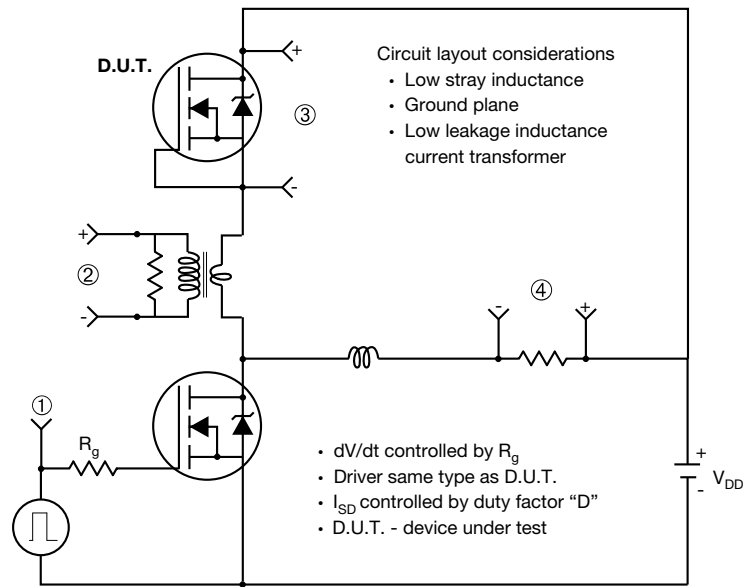


Fig. 18 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91487.



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.