# VICOR

## BCM® Bus Converter

**B048F096T24**
**B048F096M24**

RoHS  ℅ TÜV NRTL US  CE

## Narrow Input Range Sine Amplitude Converter™

- 48 V to 9.6 V VI Chip® Bus Converter
- 240 Watt (360 Watt for 1 ms)
- High density – 813 W/in³
- Small footprint – 210 W/in²
- Low weight – 0.5 oz (15 g)
- ZVS / ZCS isolated Sine Amplitude Converter™

- Typical efficiency 96%
- 125°C operation (T$_J$)
- <1 µs transient response
- 3.5 million hours MTBF
- No output filtering required

$V_{IN}$ = 38 - 55 V
$V_{OUT}$ = 7.60 - 11.0 V
$I_{OUT}$ = 25 A
K = 1/5
$R_{OUT}$ = 12.0 mΩ max
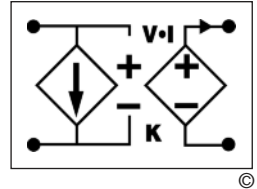
## Product Description

The VI Chip® bus converter is a high efficiency (>96%), narrow input range Sine Amplitude Converter™ (SAC™) operating from a 38 to 55 Vdc primary bus to deliver an isolated 7.60 V to 11.0 V secondary. The bus converter may be used to power non-isolated POL converters or as an independent 7.60 – 11.0 V source. Due to the fast response time and low noise of the bus converter, the need for limited life aluminum electrolytic or tantalum capacitors at the load is reduced—or eliminated—resulting in savings of board area, materials and total system cost.

The bus converter achieves a power density of 813 W/in³ in a VI Chip package compatible with standard pick-and-place and surface mount assembly process. The VI Chip package provides flexible thermal management through its low junction-to-board and junction-to-case thermal resistance. Owing to its high conversion efficiency and safe operating temperature range, the bus converter does not require a discrete heat sink in typical applications. Low junction-to-case and junction-to-lead thermal impedances assure low junction temperatures and long life in the harshest environments.
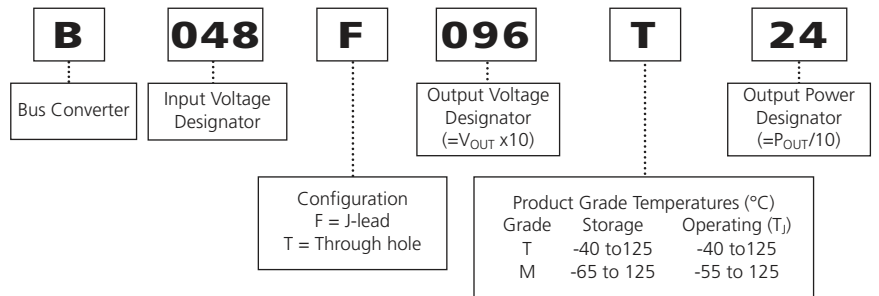
## Absolute Maximum Ratings

| Parameter | Values | Unit | Notes |
|---|---|---|---|
| +In to -In | -1.0 to 60 | Vdc | |
| | 100 | Vdc | For 100 ms |
| PC to -In | -0.3 to 7.0 | Vdc | |
| +Out to -Out | -0.5 to 16 | Vdc | |
| Isolation voltage | 2,250 | Vdc | Input to output |
| Output current | 31.5 | A | Continuous |
| Peak output current | 37.5 | A | For 1 ms |
| Output power | 240 | W | Continuous |
| Peak output power | 360 | W | For 1 ms |
| Case temperature during reflow [a] | 225 | °C | MSL 5 |
| | 245 | °C | MSL 6, TOB = 4 hrs |
| Operating junction temperature [b] | -40 to 125 | °C | T-Grade |
| | -55 to 125 | °C | M-Grade |
| Storage temperature | -40 to 125 | °C | T-Grade |
| | -65 to 125 | °C | M-Grade |

**Notes:**

[a] 245°C reflow capability applies to product with manufacturing date code 1001 and greater.

[b] The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by a shutdown comparator.

## Part Numbering

| **B** | **048** | **F** | **096** | **T** | **24** |
|---|---|---|---|---|---|
| Bus Converter | Input Voltage Designator | | Output Voltage Designator (=$V_{OUT}$ x10) | | Output Power Designator (=$P_{OUT}$/10) |

Configuration
F = J-lead
T = Through hole

| Product Grade Temperatures (°C) | | |
|---|---|---|
| Grade | Storage | Operating (T$_J$) |
| T | -40 to 125 | -40 to 125 |
| M | -65 to 125 | -55 to 125 |

BCM® Bus Converter
Page 1 of 12

Rev 5.0
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## Specifications

**Input** (Conditions are at 48 $V_{IN}$, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| Input voltage range | 38 | 48 | 55 | Vdc | |
| Input dV/dt | | | 1 | V/μs | |
| Input undervoltage turn on | | | 38.0 | Vdc | |
| Input undervoltage turn off | 32.0 | | | Vdc | |
| Input overvoltage turn on | 55.0 | | | Vdc | |
| Input overvoltage turn off | | | 60.0 | Vdc | |
| Input quiescent current | | 2.5 | | mA | PC low |
| Inrush current overshoot | | 5.3 | | A | Using test circuit in Figure 20; See Figure 1 |
| Input current | | | 5.4 | Adc | |
| Input reflected ripple current | | 140 | | mA p-p | Using test circuit in Figure 20; See Figure 4 |
| No load power dissipation | | 4.1 | 5.0 | W | |
| Internal input capacitance | | 4.0 | | μF | |
| Internal input inductance | | 5 | | nH | |
| Recommended external input capacitance | | 47 | | μF | 200 nH maximum source inductance; See Figure 20 |

## Input Waveforms
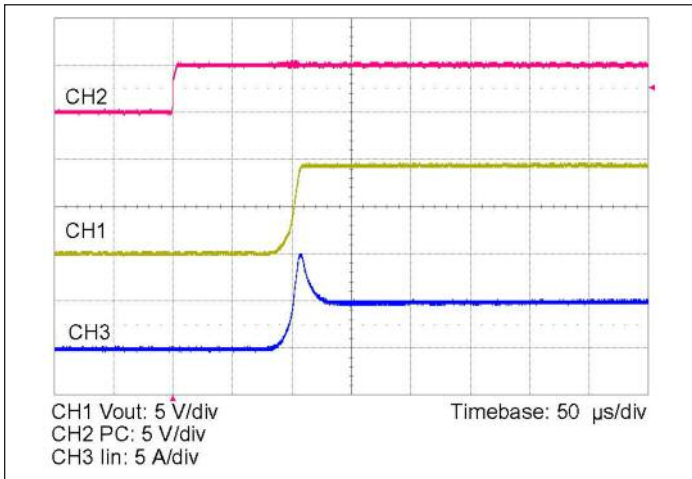


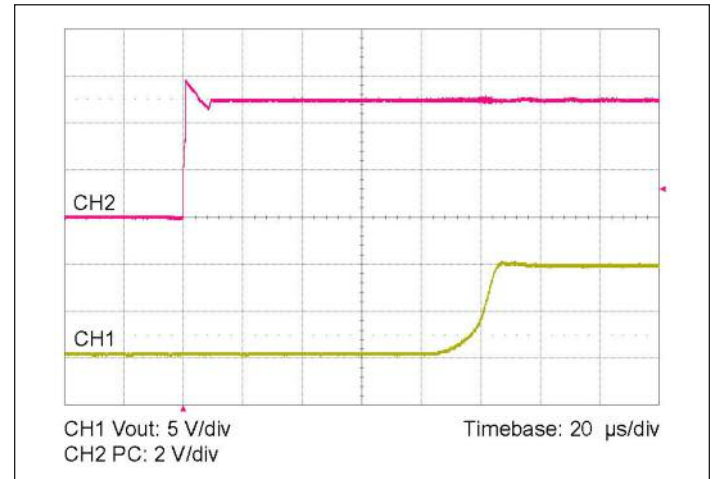*Figure 1* — *Inrush transient current at full load and 48 $V_{IN}$ with PC enabled*



*Figure 2* — *Output voltage turn on waveform with PC enabled at full load and 48 $V_{IN}$*
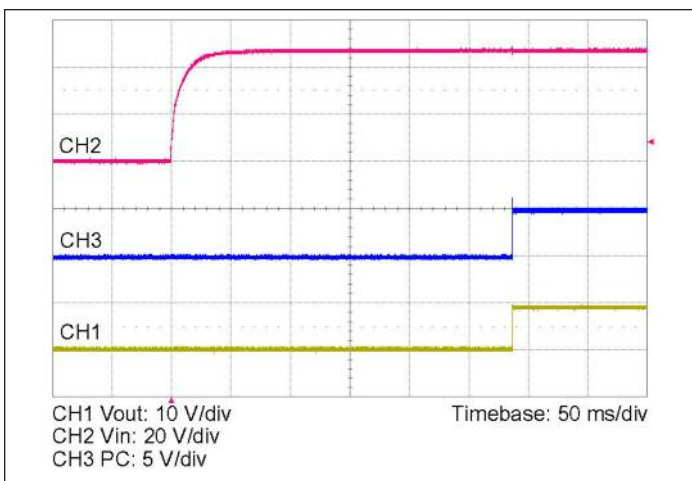


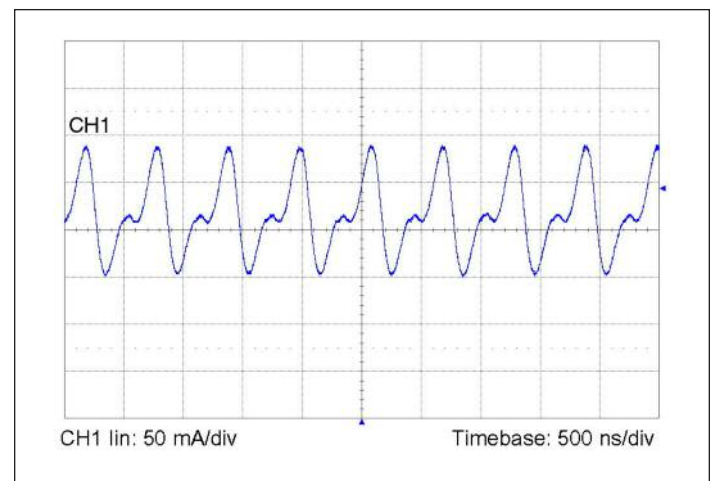*Figure 3* — *Output voltage turn on waveform with input turn on at full load and 48 $V_{IN}$*



*Figure 4* — *Input reflected ripple current at full load and 48 $V_{IN}$*

## Specifications (continued)

**Output** (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| Output voltage | 7.60 | | 11.0 | Vdc | No load |
| | 7.30 | | 10.7 | Vdc | Full load |
| Output power | 0 | | 240 | W | 40 - 55 $V_{IN}$ |
| | 0 | | 227 | W | 38 - 55 $V_{IN}$ |
| Rated DC current | 0 | | 31.5 | Adc | $P_{OUT} \leq 240$ W |
| Peak repetitive power | | | 360 | W | Max pulse width 1ms, max duty cycle 10%, baseline power 50% |
| Current share accuracy | | 5 | 10 | % | See Parallel Operation on Page 10 |
| Efficiency | | | | | |
|     Half load | 95.5 | 96.2 | | % | See Figure 5 |
|     Full load | 95.5 | 96.2 | | % | See Figure 5 |
| Internal output inductance | | 1.6 | | nH | |
| Internal output capacitance | | 55 | | µF | Effective value |
| Load capacitance | | | 1,600 | µF | |
| Output overvoltage set point | 11.0 | | | Vdc | Module will shut down |
| Output ripple voltage | | | | | |
|     No external bypass | | 176 | 200 | mVp-p | See Figures 7 and 9 |
|     10 µF bypass capacitor | | 17 | | mVp-p | See Figure 8 |
| Short circuit protection set point | 33 | | | Adc | Module will shut down |
| Average short circuit current | | 0.43 | | A | |
| Effective switching frequency | 3.0 | 3.1 | 3.4 | MHz | Fixed, 1.6 MHz per phase |
| Line regulation | | | | | |
|     K | 0.1980 | 1/5 | 0.2020 | | $V_{OUT} = K \cdot V_{IN}$ at no load |
| Load regulation | | | | | |
|     $R_{OUT}$ | | 8.9 | 12.0 | mΩ | |
| Transient response | | | | | |
|     Voltage overshoot | | 92 | | mV | 100% load step; See Figures 10 and 11 |
|     Response time | | 200 | | ns | See Figures 10 and 11 |
|     Recovery time | | 1 | | µs | See Figures 10 and 11 |
| Output overshoot | | | | | |
|     Input turn on | | 0 | | mV | No output filter; See Figure 3 |
|     PC enable | | 0 | | mV | No output filter; See Figure 2 |
| Output turn on delay | | | | | |
|     From application of power | | 288 | | ms | No output filter; See Figure 3 |
|     From release of PC pin | | 70 | | ms | No output filter |

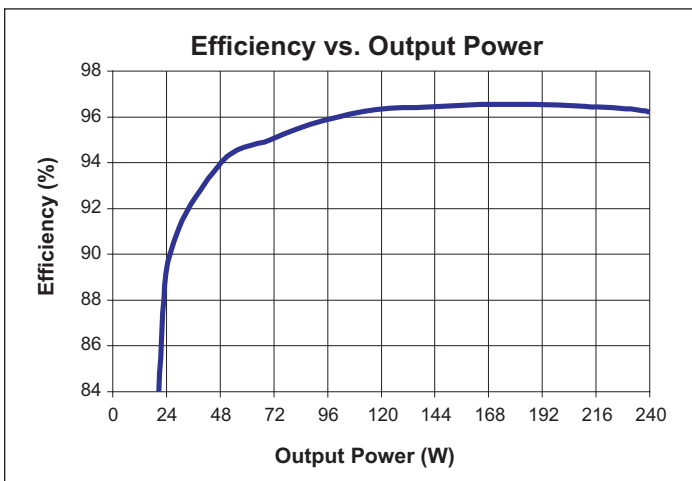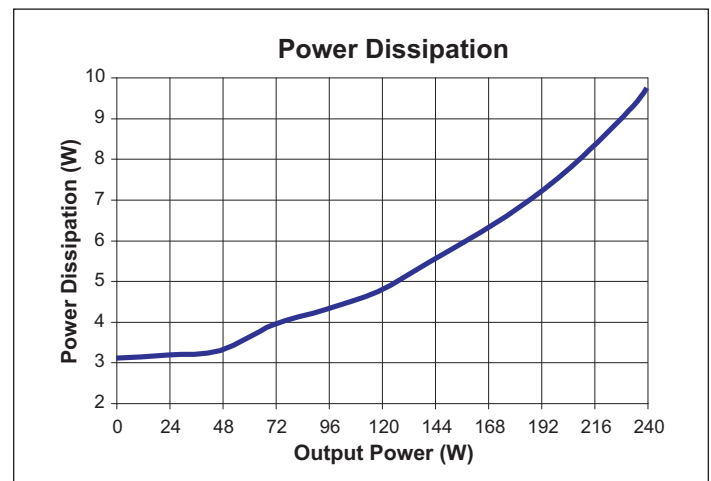## Output Waveforms



Figure 5 — Efficiency vs. output power



Figure 6 — Power dissipation as a function of output power
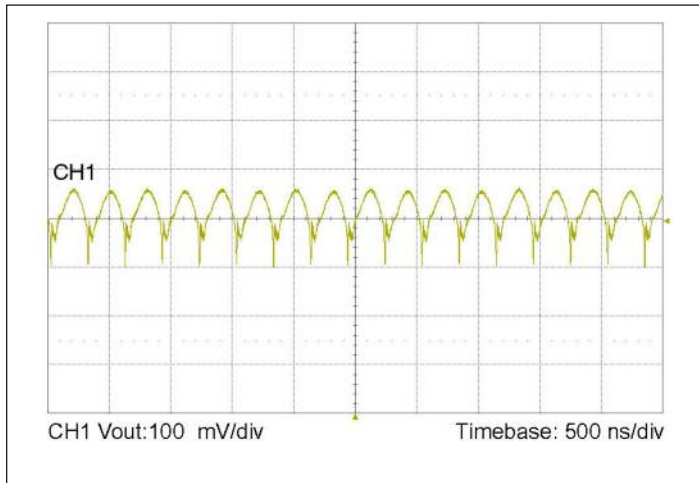
## Specifications (continued)

## Output Waveforms



CH1

CH1 Vout:100 mV/div          Timebase: 500 ns/div

*Figure 7* — *Output voltage ripple at full load and 48 $V_{IN}$ without any external bypass capacitor.*
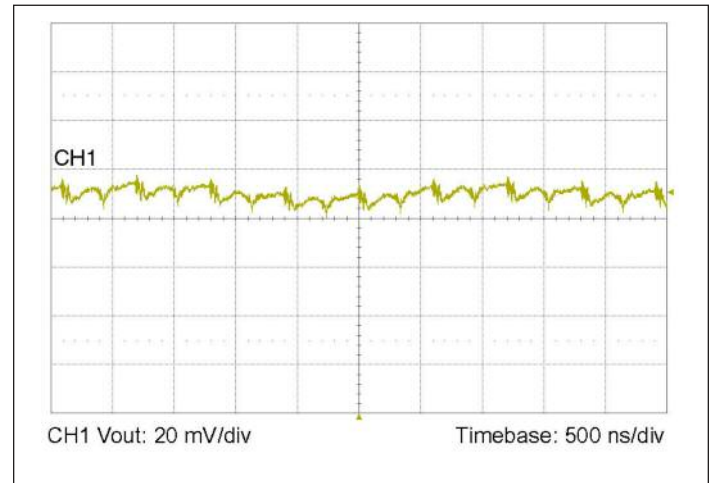


CH1

CH1 Vout: 20 mV/div          Timebase: 500 ns/div

*Figure 8* — *Output voltage ripple at full load and 48 $V_{IN}$ with 10 µF ceramic external bypass capacitor and 20 nH of distribution inductance.*
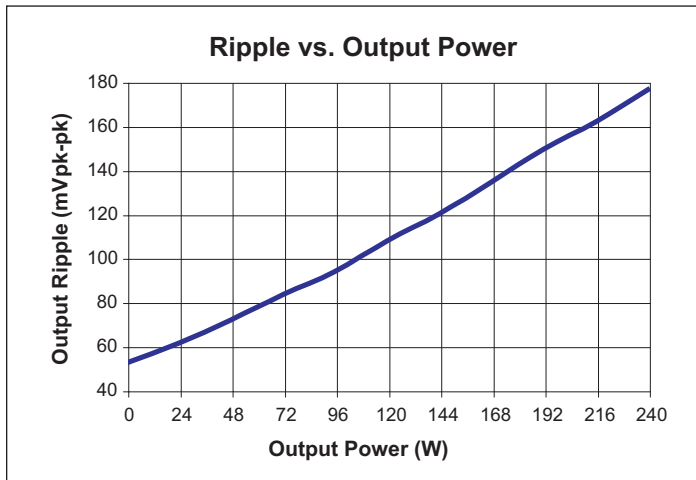


**Ripple vs. Output Power**

Output Ripple (mVpk-pk)

Output Power (W)

*Figure 9* — *Output voltage ripple vs. output power at 48 $V_{IN}$ without any external bypass capacitor.*



CH1

CH2

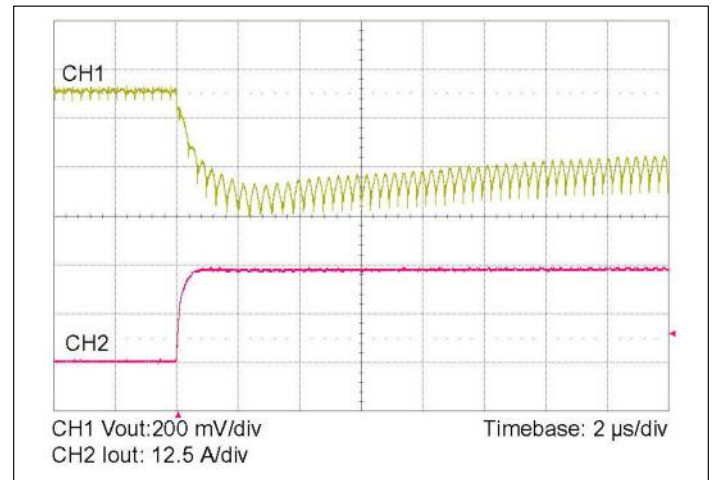CH1 Vout:200 mV/div          Timebase: 2 µs/div
CH2 Iout: 12.5 A/div

*Figure 10* — *0 – 25 A load step with 100 µF input capacitor and no output capacitor.*



CH1

CH2

CH1 Vout: 200 mV/div          Timebase: 2 µs/div
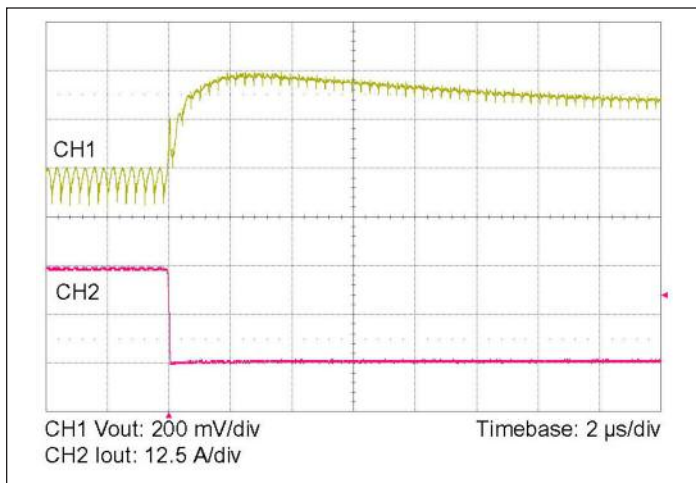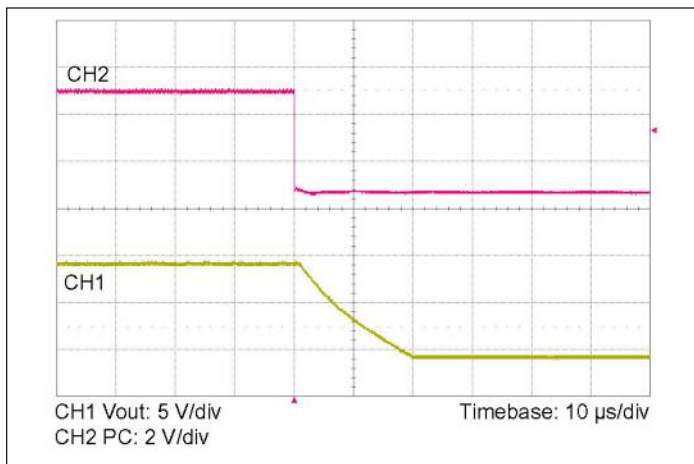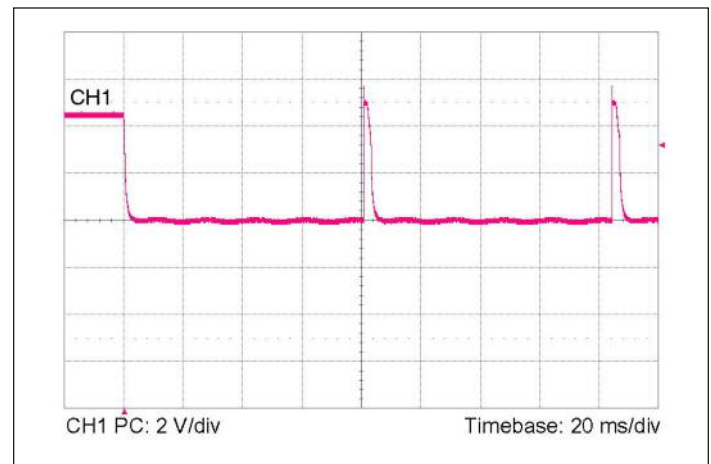CH2 Iout: 12.5 A/div

*Figure 11* — *25 – 0 A load step with 100 µF input capacitor and no output capacitor.*

## Specifications (continued)

### General

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| MTBF | | | | | |
| MIL-HDBK-217F | | 3.5 | | Mhrs | 25°C, GB |
| Isolation specifications | | | | | |
| Voltage | 2,250 | | | Vdc | Input to output |
| Capacitance | | 3,000 | | pF | Input to output |
| Resistance | 10 | | | MΩ | Input to output |
| | | cTÜVus | | | UL/CSA 60950-1, EN 60950-1 |
| Agency approvals | | CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable | | | |
| Mechanical | | | | | See mechanical drawings, Figures 15 – 18 |
| Weight | | 0.53/15 | | oz/g | |
| Dimensions | | | | | |
| Length | | 1.28/32,5 | | in/mm | |
| Width | | 0.87/22 | | in/mm | |
| Height | | 0.265/6,73 | | in/mm | |
| Thermal | | | | | |
| Overtemperature shutdown | 125 | 130 | 135 | °C | Junction temperature |
| Thermal capacity | | 9.3 | | Ws/°C | |
| Junction-to-case thermal impedance ($R_{\theta JC}$) | | 1.1 | | °C/W | See Thermal Considerations on Page 10 |
| Junction-to-board thermal impedance ($R_{\theta JB}$) | | 2.1 | | °C/W | |

### Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| Primary control (PC) | | | | | |
| DC voltage | 4.8 | 5.0 | 5.2 | Vdc | |
| Module disable voltage | 2.4 | 2.5 | | Vdc | |
| Module enable voltage | | 2.5 | 2.6 | Vdc | |
| Current limit | 2.4 | 2.5 | 2.9 | mA | Source only |
| Enable delay time | | 70 | | ms | |
| Disable delay time | | 20 | | µs | See Figure 12, time from PC low to output low |



CH1 Vout: 5 V/div
CH2 PC: 2 V/div
Timebase: 10 µs/div

*Figure 12* — $V_{OUT}$ at full load vs. PC disable



CH1 PC: 2 V/div
Timebase: 20 ms/div

*Figure 13* — PC signal during fault

**BCM® Bus Converter**
Page 5 of 12

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## Pin / Control Functions

### +In / -In – DC Voltage Input Ports

The VI Chip module input voltage range should not be exceeded. An internal undervoltage/overvoltage lockout function prevents operation outside of the normal operating input range. The BCM® bus converter turns on within an input voltage window bounded by the "Input undervoltage turn on" and "Input overvoltage turn off" levels, as specified. The module may be protected against accidental application of a reverse input voltage by the addition of a rectifier in series with the positive input, or a reverse rectifier in shunt with the positive input located on the load side of the input fuse.

The connection of the module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be 47 µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

### PC – Primary Control

The Primary Control port is a multifunction node that provides the following functions:

Enable / Disable – If the PC port is left floating, the BCM module output is enabled. Once this port is pulled lower than 2.4 Vdc with respect to –In, the output is disabled. This action can be realized by employing a relay, opto-coupler, or open collector transistor. Refer to Figures 1-3, 12 and 13 for the typical enable/disable characteristics. This port should not be toggled at a rate higher than 1 Hz. The PC port should also not be driven by or pulled up to an external voltage source.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5.0 Vdc. The PC port should never be used to sink current.

Alarm – The module contains circuitry that monitors output overload, input overvoltage or undervoltage, and internal junction temperatures. In response to an abnormal condition in any of the monitored parameters, the PC port will toggle. Refer to Figure 13 for PC alarm characteristics.

### TM and RSV – Reserved for factory use.

### +Out / -Out – DC Voltage Output Ports

Two sets of contacts are provided for the +Out port. They must be connected in parallel with low interconnect resistance. Similarly, two sets of contacts are provided for the –Out port. They must be connected in parallel with low interconnect resistance. Within the specified operating range, the average output voltage is defined by the Level 1 DC behavioral model of Figure 21. The current source capability of the module is rated in the specifications section of this document.

The low output impedance of the module reduces or eliminates the need for limited life aluminum electrolytic or tantalum capacitors at the input of POL converters.

Total load capacitance at the output of the modules should not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the module, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the BCM module.



Bottom View

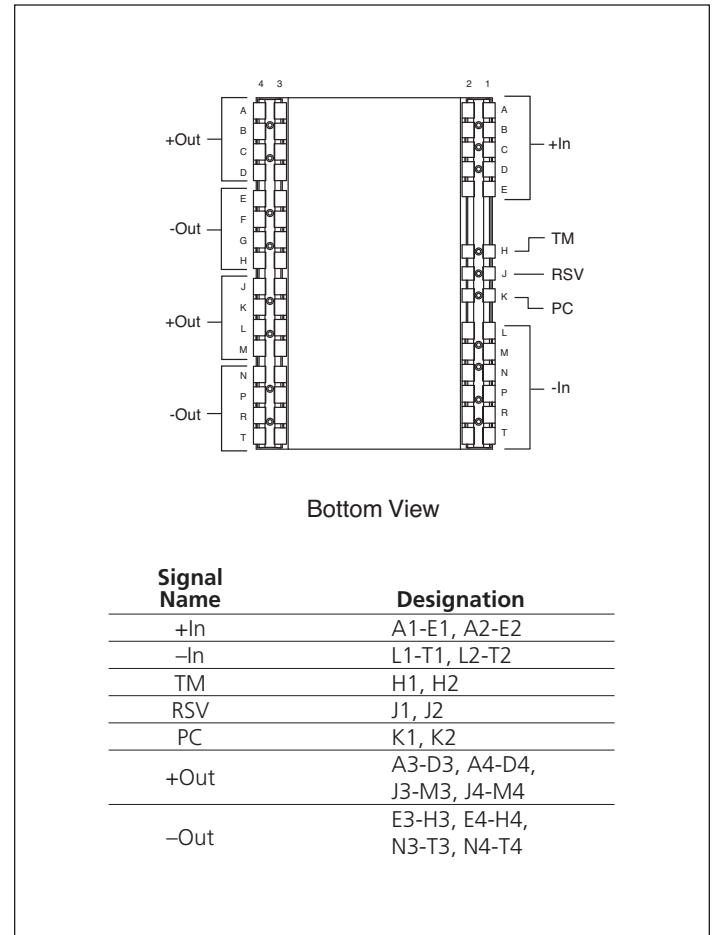| Signal Name | Designation |
|---|---|
| +In | A1-E1, A2-E2 |
| –In | L1-T1, L2-T2 |
| TM | H1, H2 |
| RSV | J1, J2 |
| PC | K1, K2 |
| +Out | A3-D3, A4-D4, J3-M3, J4-M4 |
| –Out | E3-H3, E4-H4, N3-T3, N4-T4 |

**Figure 14** — *BCM® bus converter pin configuration*

## Mechanical Drawings
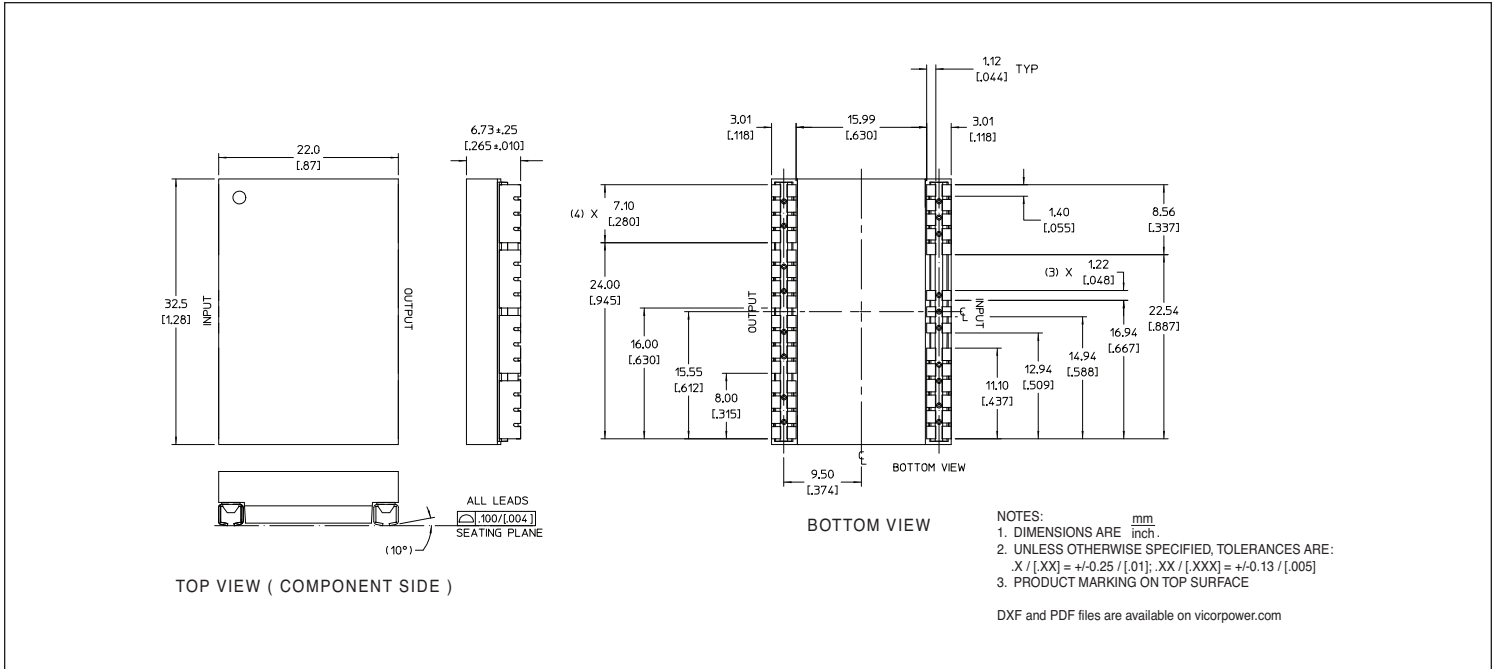


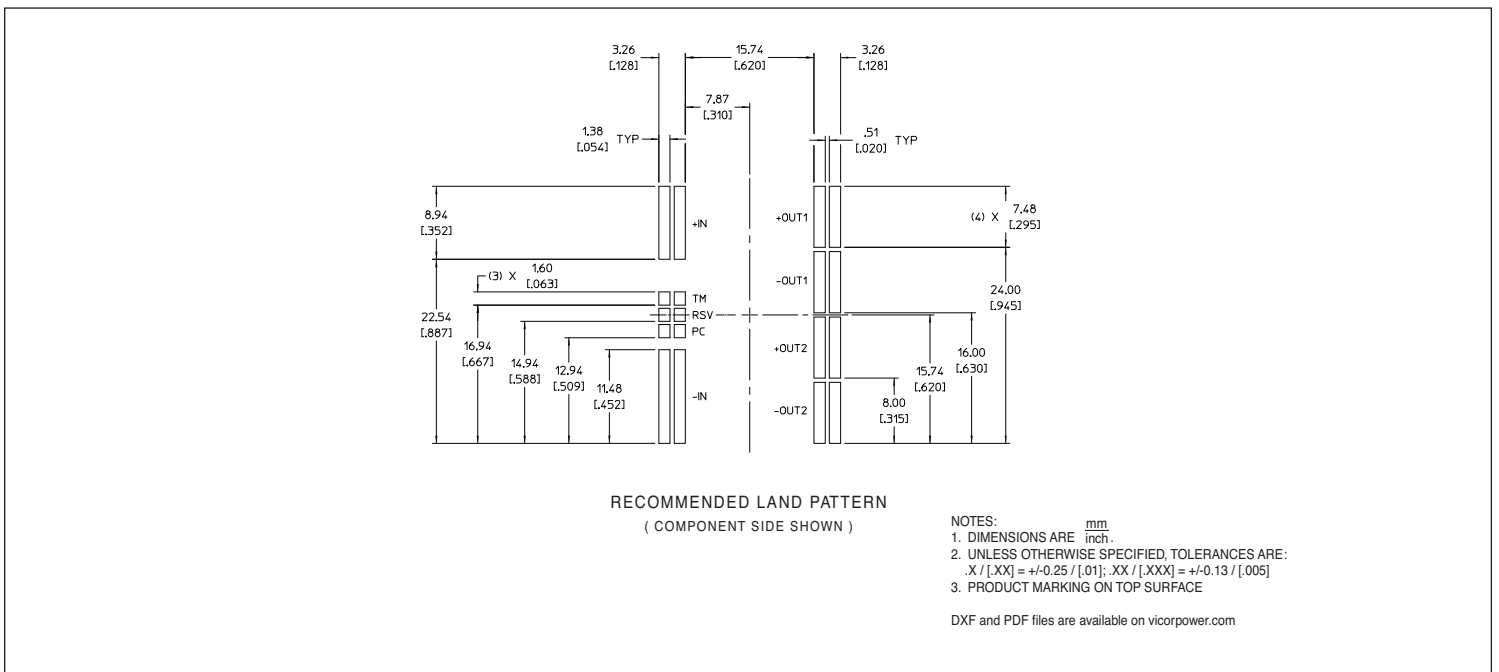*Figure 15* — *BCM® module J-Lead mechanical outline; onboard mounting*

NOTES:
1. DIMENSIONS ARE $\frac{mm}{inch}$.
2. UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
   .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
3. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com



*Figure 16* — *BCM module PCB land layout information*

RECOMMENDED LAND PATTERN
( COMPONENT SIDE SHOWN )

NOTES:
1. DIMENSIONS ARE $\frac{mm}{inch}$.
2. UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
   .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
3. PRODUCT MARKING ON TOP SURFACE

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**BCM® Bus Converter**
Page 7 of 12

Rev 5.0
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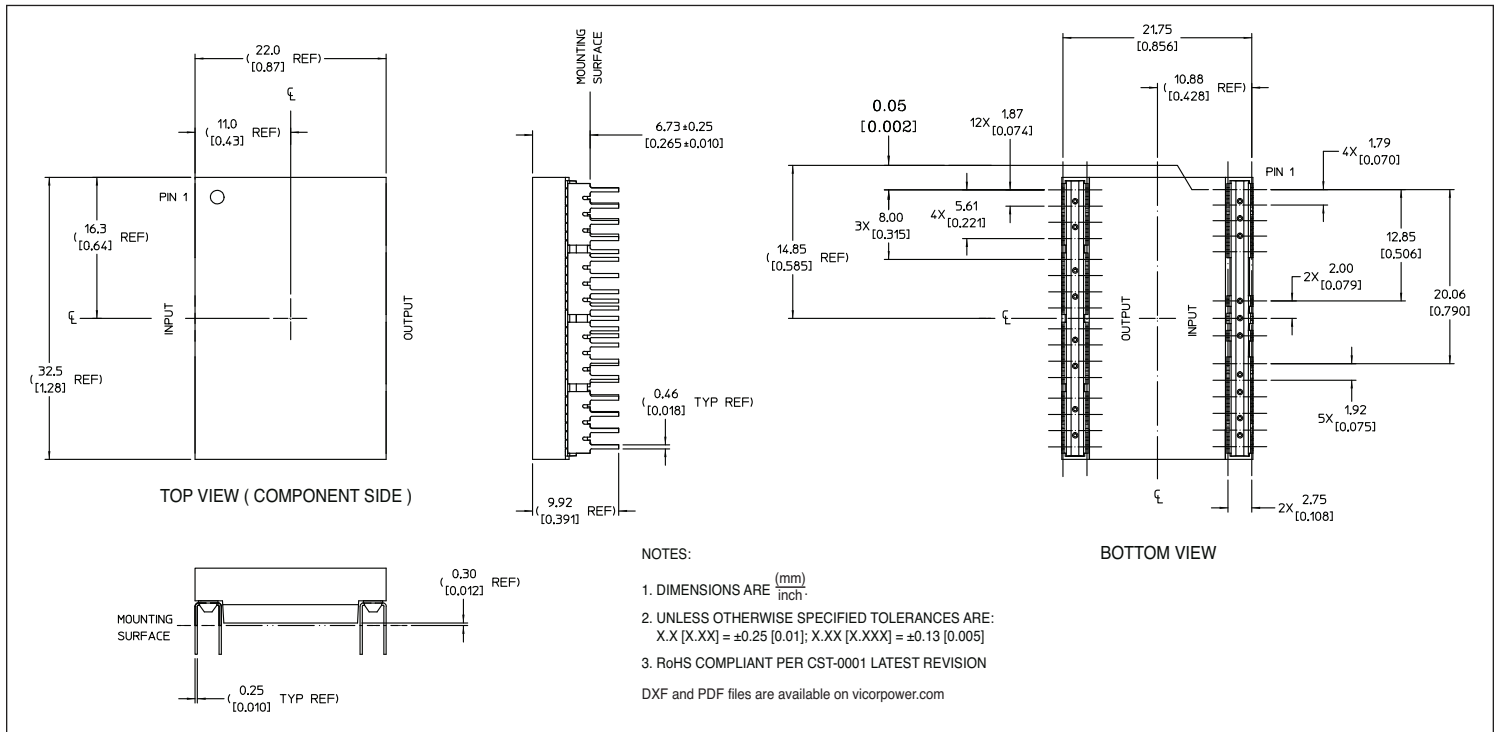
## Mechanical Drawings (continued)



*Figure 17* — *BCM® through-hole module mechanical outline*
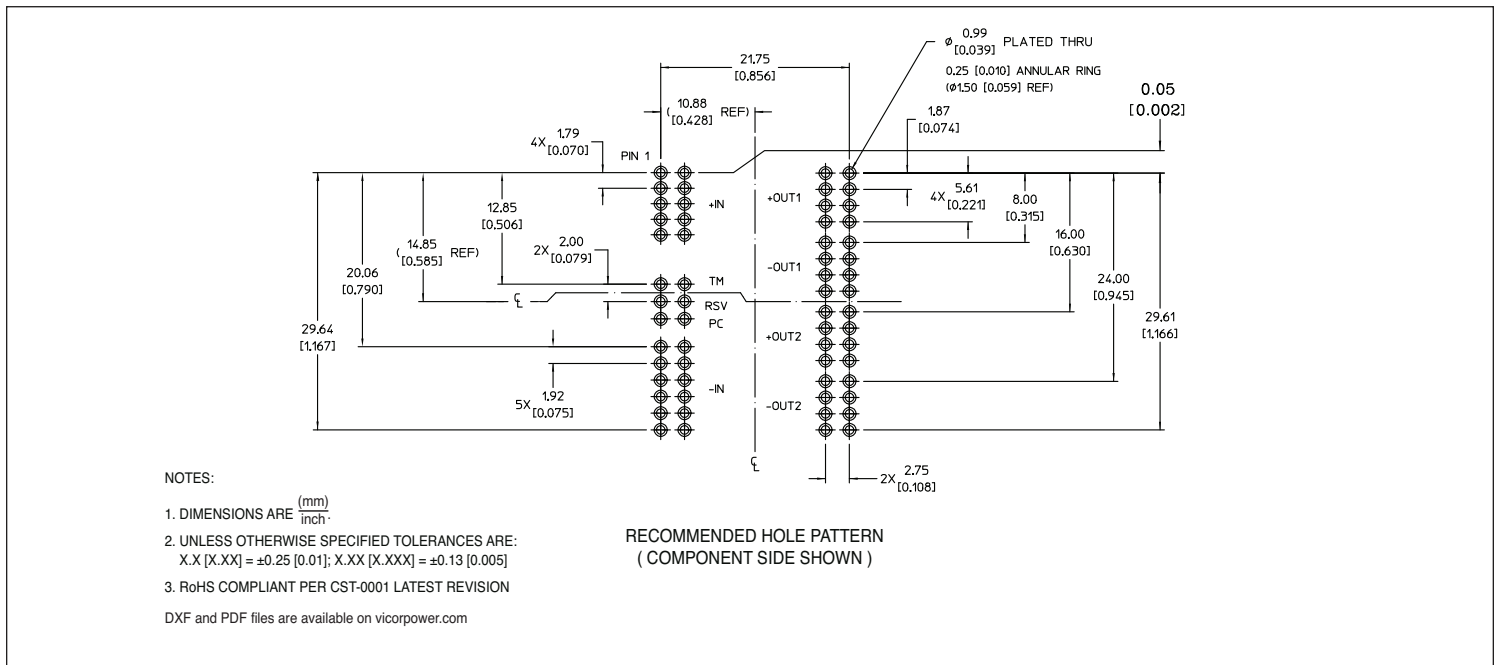


*Figure 18* — *BCM through-hole module PCB layout information*

## Configuration Options



RECOMMENDED LAND PATTERN
(NO GROUNDING CLIPS)
TOP SIDE SHOWN

RECOMMENDED LAND PATTERN
(With GROUNDING CLIPS)
TOP SIDE SHOWN

NOTES: 1. MAINTAIN 3.50 [0.138] DIA. KEEP-OUT ZONE
FREE OF COPPER, ALL PCB LAYERS.

2. (A) MINIMUM RECOMMENDED PITCH IS 39.50 [1.555],
THIS PROVIDES 7.00 [0.275] COMPONENT
EDGE-TO-EDGE SPACING, AND 0.50 [0.020]
CLEARANCE BETWEEN VICOR HEAT SINKS.

(B) MINIMUM RECOMMENDED PITCH IS 41.00 [1.614],
THIS PROVIDES 8.50 [0.334] COMPONENT
EDGE-TO-EDGE SPACING, AND 2.00 [0.079]
CLEARANCE BETWEEN VICOR HEAT SINKS.

3. VI CHIP® MODULE LAND PATTERN SHOWN FOR REFERENCE ONLY;
ACTUAL LAND PATTERN MAY DIFFER.
DIMENSIONS FROM EDGES OF LAND PATTERN
TO PUSH-PIN HOLES WILL BE THE SAME FOR
ALL FULL SIZE VI CHIP PRODUCTS.

4. RoHS COMPLIANT PER CST-0001 LATEST REVISION.

5. UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE MM [INCH].
TOLERANCES ARE:
X.X [X.XX] = ±0.3 [0.01]
X.XX [X.XXX] = ±0.13 [0.005]

6. PLATED THROUGH HOLES FOR GROUNDING CLIPS (33855)
SHOWN FOR REFERENCE. HEAT SINK ORIENTATION AND
DEVICE PITCH WILL DICTATE FINAL GROUNDING SOLUTION.
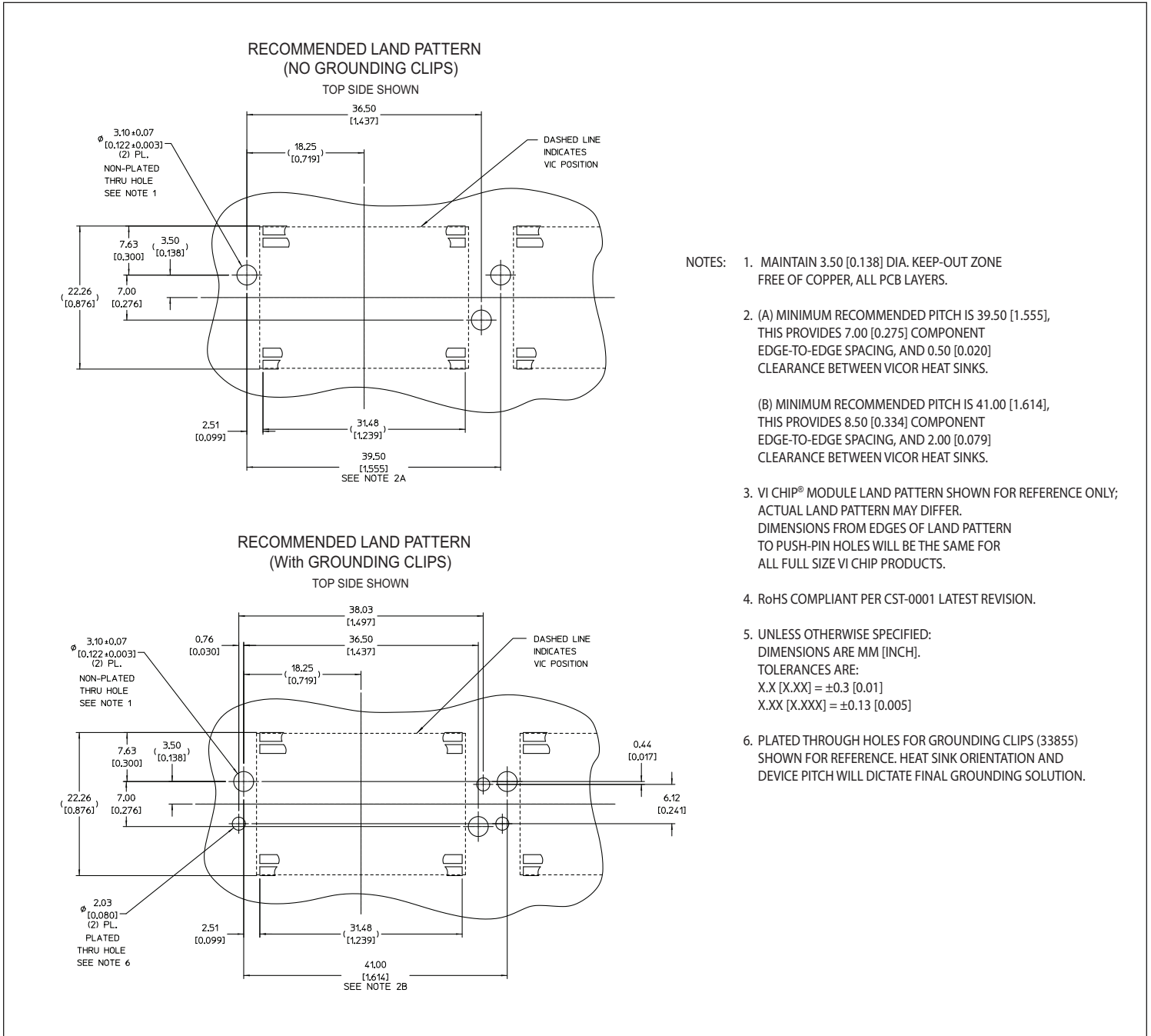
*Figure 19* — *Hole location for push pin heat sink relative to VI Chip® module*

## Application Note

### Parallel Operation

The BCM® bus converter will inherently current share when operated in an array. Arrays may be used for higher power or redundancy in an application.

Current sharing accuracy is maximized when the source and load impedance presented to each bus converter within an array are equal. The recommended method to achieve matched impedances is to dedicate common copper planes within the PCB to deliver and return the current to the array, rather than rely upon traces of varying lengths. In typical applications the current being delivered to the load is larger than that sourced from the input, allowing traces to be utilized on the input side if necessary. The use of dedicated power planes is, however, preferable.

The bus converter power train and control architecture allow bi-directional power transfer, including reverse power processing from the module output to its input. Reverse power transfer is enabled if the module input is within its operating range and the module is otherwise enabled. The bus converter's ability to process power in reverse improves the module's transient response to an output load dump.

### Thermal Considerations

VI Chip products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input/output conditions, thermal management and environmental conditions. Maintaining the top of the B048F096T24 case to less than 100°C will keep all junctions within the module below 125°C for most applications. The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.
It is not recommended to use a module for an extended period of time at full load without proper heat sinking.

### Input Impedance Recommendations

To take full advantage of the BCM bus converter capabilities, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The source should exhibit low inductance and should have a critically damped response. If the interconnect inductance is excessive, the module input pins should be bypassed with an RC damper (e.g., 47 µF in series with 0.3 ohm) to retain low source impedance and proper operation. Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response.

Anomalies in the response of the source will appear at the output of the module multiplied by its K factor. The DC resistance of the source should be kept as low as possible to minimize voltage deviations. This is especially important if the module is operated near low or high line as the overvoltage/undervoltage detection circuitry could be activated.

### Input Fuse Recommendations

VI Chip modules are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of the modules must always be incorporated within the power system. A fast acting fuse should be placed in series with the +In port.
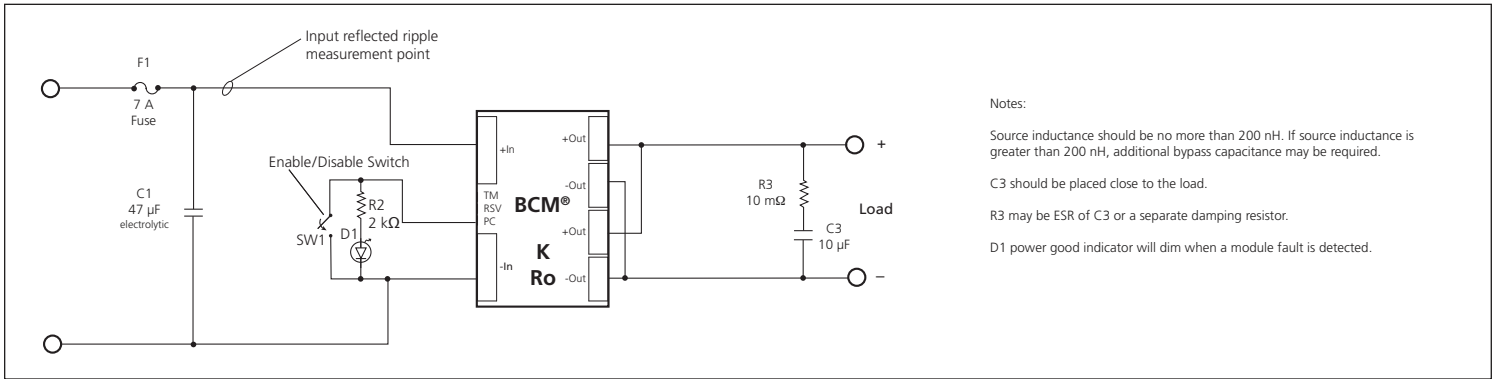
## Application Note (continued)



***Figure 20*** — *BCM® module test circuit*

Notes:

Source inductance should be no more than 200 nH. If source inductance is greater than 200 nH, additional bypass capacitance may be required.

C3 should be placed close to the load.

R3 may be ESR of C3 or a separate damping resistor.

D1 power good indicator will dim when a module fault is detected.

## BCM® Bus Converter Level 1 DC Behavioral Model for 48 V to 9.6 V, 240 W
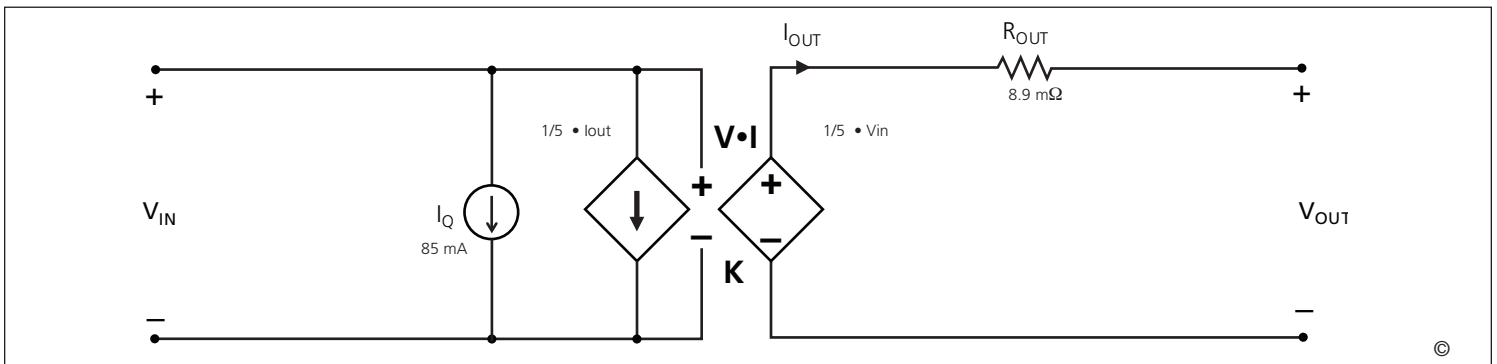


***Figure 21*** — *This model characterizes the DC operation of the bus converter, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

## BCM® Bus Converter Level 2 Transient Behavioral Model for 48 V to 9.6 V, 240 W
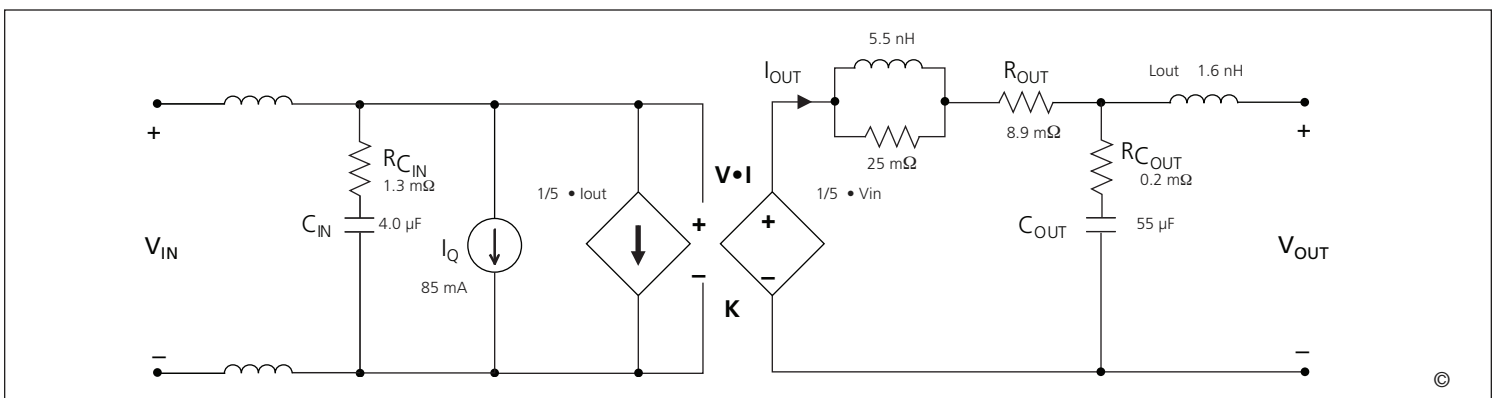


***Figure 22*** — *This model characterizes the AC operation of the bus converter including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

**BCM® Bus Converter**
Page 11 of 12

Rev 5.0
06/2014

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**Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.**

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