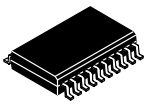
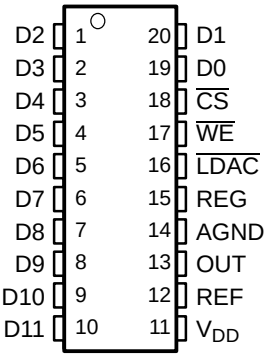


2.7-V TO 5.5-V LOW-POWER 12-BIT DIGITAL-TO-ANALOG CONVERTERS WITH INTERNAL REFERENCE AND POWER DOWN

FEATURES

- **12-Bit Voltage Output DAC**
- **Programmable Internal Reference**
- **Programmable Settling Time vs Power Consumption**
  - **1 µs in Fast Mode**
  - **3.5 µs in Slow Mode**
- **Compatible With TMS320**
- **Differential Nonlinearity . . . <0.5 LSB Typ**
- **Voltage Output Range . . . 2x the Reference Voltage**
- **Monotonic Over Temperature**

DW OR PW PACKAGE
(TOP VIEW)



APPLICATIONS

- **Digital Servo Control Loops**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Control**
- **Machine and Motion Control Devices**
- **Mass Storage Devices**

DESCRIPTION

The TLV5639 is a 12-bit voltage output digital-to-analog converter (DAC) with a microprocessor compatible parallel interface. It is programmed with a 16-bit data word containing 4 control and 12 data bits. Developed for a wide range of supply voltages, the TLV5639 can be operated from 2.7 V to 5.5 V.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation. Because of its ability to source up to 1 mA, the internal reference can also be used as a system reference. With its on-chip programmable precision voltage reference, the TLV5639 simplifies overall system design. The settling time and the reference voltage can be chosen by the control bits within the 16-bit data word.

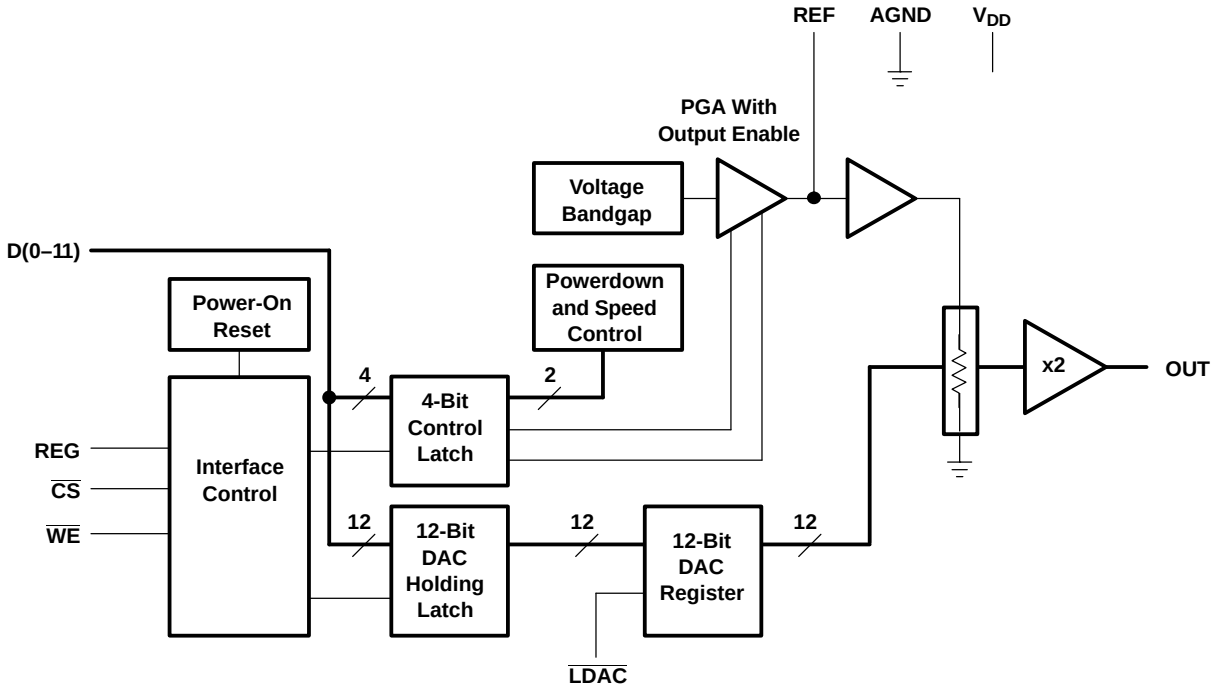
Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in 20-pin SOIC and TSSOP packages in standard commercial and industrial temperature ranges.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SOIC (DW)	TSSOP (PW)
0°C to 70°C	TLV5639CDW	TLV5639CPW
-40°C to 85°C	TLV5639IDW	TLV5639IPW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O/P	DESCRIPTION
AGND	14	P	Ground
$\overline{CS}$	18	I	Chip select. Digital input active low, used to enable/disable inputs
D0-D11	1-10, 19, 20	I	Data input
$\overline{LDAC}$	16	I	Load DAC. Digital input active low, used to load DAC output
OUT	13	O	DAC analog voltage output
REG	15	I	Register select. Digital input, used to access control register
REF	12	I/O	Analog reference voltage input/output
V_{DD}	11	P	Positive power supply
$\overline{WE}$	17	I	Write enable. Digital input active low, used to latch data

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
Supply voltage (V_{DD} to AGND)		7 V
Reference input voltage range		- 0.3 V to V_{DD} + 0.3 V
Digital input voltage range		- 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A	TLV5639C	0°C to 70°C
	TLV5639I	-40°C to 85°C
Storage temperature range, T_{stg}		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 5 V	4.5	5	5.5	V
	V_{DD} = 3 V	2.7	3	3.3	V
Power on threshold voltage, POR		0.55		2	V
High-level digital input voltage, V_{IH}	V_{DD} = 2.7 V	2			V
	V_{DD} = 5.5 V	2.4			
Low-level digital input voltage, V_{IL}	V_{DD} = 2.7 V			0.6	V
	V_{DD} = 5.5 V			1	
Reference voltage, V_{ref} to REF terminal	V_{DD} = 5 V (1)	AGND	2.048	V_{DD}-1.5	V
Reference voltage, V_{ref} to REF terminal	V_{DD} = 3 V (1)	AGND	1.024	V_{DD}-1.5	V
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Operating free-air temperature, T_A	TLV5639C	0		70	°C
	TLV5639I	40		85	

(1) Due to the x2 output buffer, a reference input voltage ≥ $V_{DD/2}$ causes clipping of the transfer function. The output buffer of the internal reference must be disabled, if an external reference is used.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

POWER SUPPLY									
PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	V_{DD}= 5 V	REF on	Fast		2.3	2.8	mA
					Slow		1.3	1.6	mA
				REF off	Fast		1.9	2.4	mA
					Slow		0.9	1.2	mA
			V_{DD} = 3 V	REF on	Fast		2.1	2.6	mA
					Slow		1.2	1.5	mA
				REF off	Fast		1.8	2.3	mA
					Slow		0.9	1.1	mA
	Power down supply current						0.01	1	µA
PSRR	Power supply rejection ratio	Zero scale, External reference (1)					60		dB
		Full scale, External reference (2)					60		

(1) Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
PSRR = 20 log [(E_{ZS}(V_{DD}max) - E_{ZS}(V_{DD}min))/V_{DD}max]
(2) Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
PSRR = 20 log [(E_G(V_{DD}max) - E_G(V_{DD}min))/V_{DD}max]

STATIC DAC SPECIFICATIONS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			12		bits
INL	Integral nonlinearity, end point adjusted	R_L = 10 kΩ, C_L = 100 pF, See note (1)		±1.2	±3	LSB
DNL	Differential nonlinearity	R_L = 10 kΩ, C_L = 100 pF, See note (2)		±0.3	±0.5	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	See note (3)			±12	LSB
E_{ZS}TC	Zero-scale-error temperature coefficient	See note (4)		20		ppm/°C
E_G	Gain error	See note (5)			±0.3	% full scale V
E_GTC	Gain error temperature coefficient	See note (6)		20		ppm/°C

(1) The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text).
(2) The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
(3) Zero-scale error is the deviation from zero voltage output when the digital input code is zero (see text).
(4) Zero-scale-error temperature coefficient is given by: E_{ZS} TC = [E_{ZS} (T_{max}) - E_{ZS} (T_{min})]/2V_{ref}× 10^6/(T_{max} - T_{min}).
(5) Gain error is the deviation from the ideal output (2V_{ref} - 1 LSB) with an output load of 10 k excluding the effects of the zero-error.
(6) Gain temperature coefficient is given by: E_G TC = [E_G(T_{max}) - E_G (T_{min})]/2V_{ref}× 10^6/(T_{max} - T_{min}).

OUTPUT SPECIFICATIONS					
PARAMETER		TEST CONDITIONS	MIN TYP	MAX	UNIT
V_O	Output voltage	R_L = 10 kΩ		V_{DD}-0.4	V
	Output load regulation accuracy	V_O= 4.096 V, 2.048 V, R_L = 2 kΩ		±0.29	% full scale V

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

REFERENCE PIN CONFIGURED AS OUTPUT (REF)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ref(OUTL)}$	Low reference voltage		1.003	1.024	1.045	V
$V_{ref(OUTH)}$	High reference voltage	V_{DD} > 4.75 V	2.027	2.048	2.069	V
$I_{ref(source)}$	Output source current				1	mA
$I_{ref(sink)}$	Output sink current		1			mA
PSRR	Power supply rejection ratio			48		dB

REFERENCE PIN CONFIGURED AS INPUT (REF)							
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_I	Input voltage				0		V_{DD}- 1.5	V
R_I	Input resistance					10		MΩ
C_I	Input capacitance					5		pF
	Reference input bandwidth	REF = 0.2 V_{pp} + 1.024 V dc		Fast		900		kHz
				Slow		500		
	Harmonic distortion, reference input	REF = 1 V_{pp} + 2.048 V dc, V_{DD} = 5 V	10 kHz	Fast		87		dB
				Slow		77		
			50 kHz	Fast		74		dB
				Slow		61		
			100 kHz	Fast		66		dB
	Reference feedthrough	REF = 1 V_{pp} at 1 kHz + 1.024 V dc, See (1)				80		dB

(1) Reference feedthrough is measured at the DAC output with an input code = 0x000.

DIGITAL INPUTS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			1	µA
I_{IL}	Low-level digital input current	V_I = 0 V	1			µA
C_i	Input capacitance			8		pF

OPERATING CHARACTERISTICS

over recommended operating free-air temperature range, V_{ref} = 2.048 V, and V_{ref} = 1.024 V, (unless otherwise noted)

ANALOG OUTPUT DYNAMIC PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	R_L = 10 kΩ, C_L = 100 pF, see note (1)	Fast		1	3	µs
			Slow		3.5	7	
$t_{s(CC)}$	Output settling time, code to code	R_L = 10 kΩ, C_L = 100 pF, see note (2)	Fast		0.5	1.5	µs
			Slow		1	2	
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, see note (3)	Fast	6	10		V/µs
			Slow	1.2	1.7		
	Glitch energy	DIN = 0 to 1, f_{CLK} = 100 kHz, $\overline{CS}$ = V_{DD}			5		nV-S
SNR	Signal-to-noise ratio	f_s = 480 kSPS, f_B = 20 kHz, C_L = 100 pF, f_{out} = 1 kHz, R_L = 10 kΩ,		73	78		dB
SINAD	Signal-to-noise + distortion			61	67		
THD	Total harmonic distortion				69	62	
SFDR	Spurious free dynamic range			63	74		

(1) Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDF or 0xFDF to 0x020.
(2) Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count.
(3) Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

DIGITAL INPUT TIMING REQUIREMENTS

		MIN	NOM	MAX	UNIT
$t_{su(CS-WE)}$	Setup time, $\overline{CS}$ low before negative $\overline{WE}$ edge	15			ns
$t_{su(D)}$	Setup time, data ready before positive $\overline{WE}$ edge	10			ns
$t_{su(R)}$	Setup time, REG ready before positive $\overline{WE}$ edge	20			ns
$t_{h(DR)}$	Hold time, data and REG held valid after positive $\overline{WE}$ edge	5			ns
$t_{su(WE-LD)}$	Setup time, positive $\overline{WE}$ edge before $\overline{LDAC}$ low	5			ns
$t_{wH(WE)}$	Pulse duration, $\overline{WE}$ high	20			ns
$t_{w(LD)}$	Pulse duration, $\overline{LDAC}$ low	23			ns

PARAMETER MEASUREMENT INFORMATION

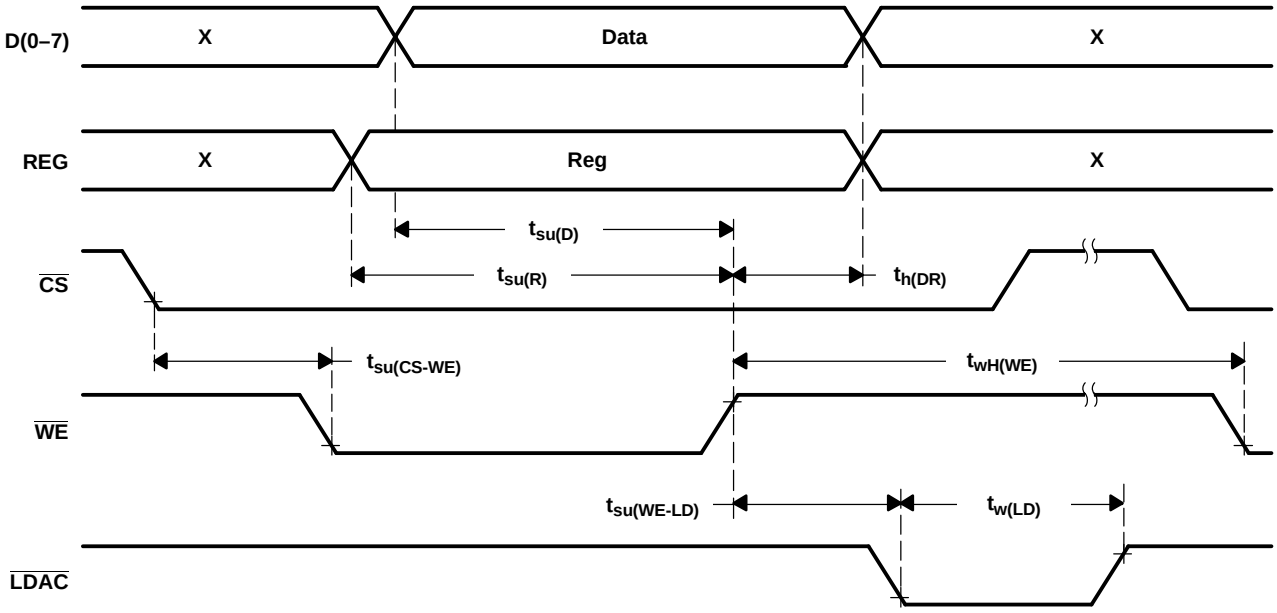


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

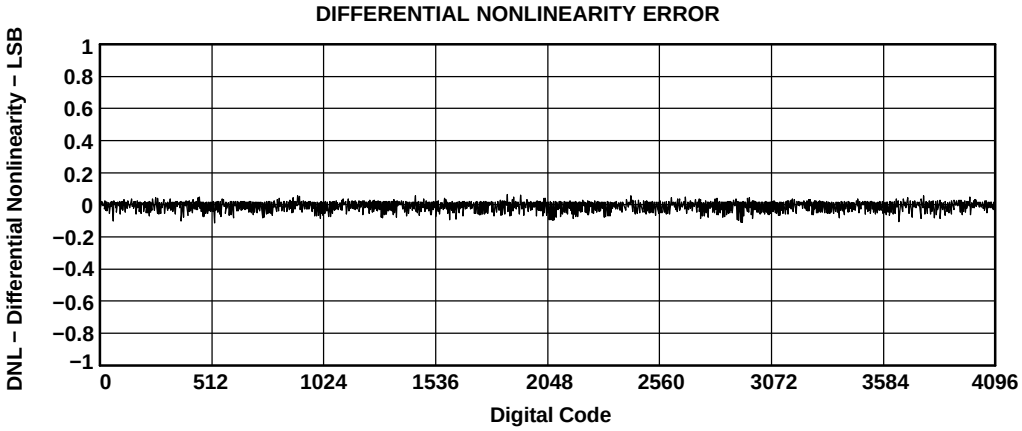


Figure 2.

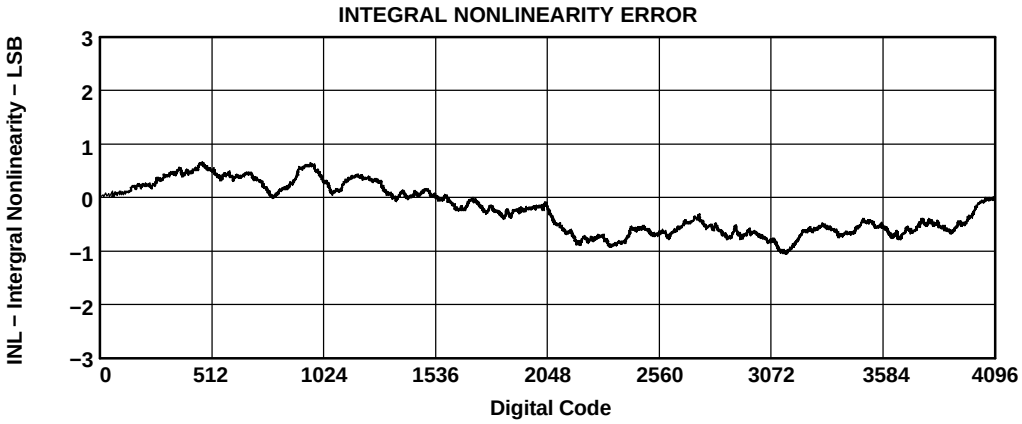


Figure 3.

TYPICAL CHARACTERISTICS (continued)

MAXIMUM OUTPUT VOLTAGE
vs
LOAD CURRENT

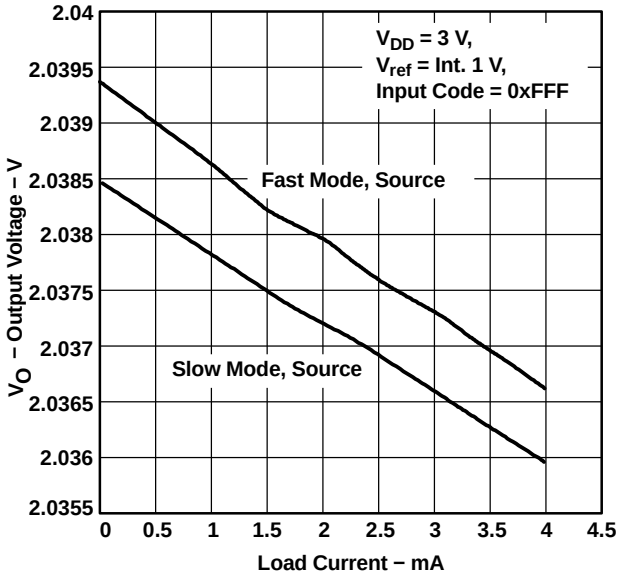


Figure 4.

MAXIMUM OUTPUT VOLTAGE
vs
LOAD CURRENT

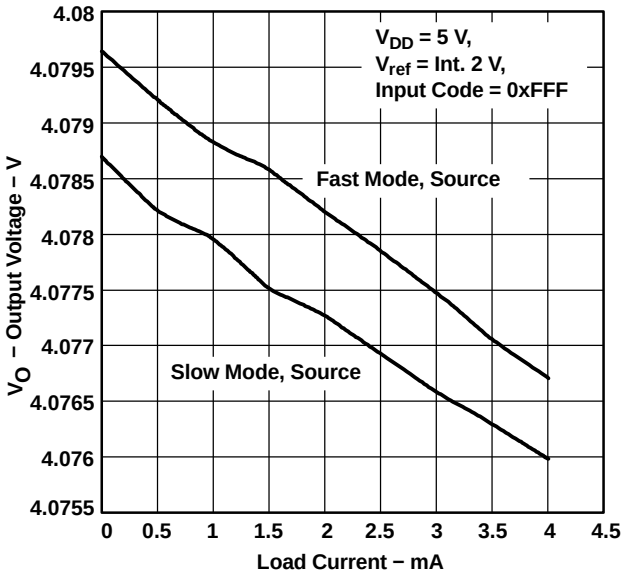


Figure 5.

MINIMUM OUTPUT VOLTAGE
vs
LOAD CURRENT

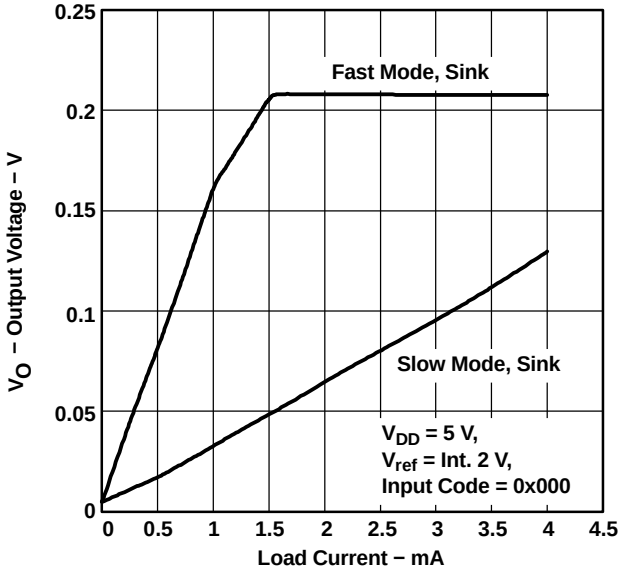


Figure 6.

MINIMUM OUTPUT VOLTAGE
vs
LOAD CURRENT

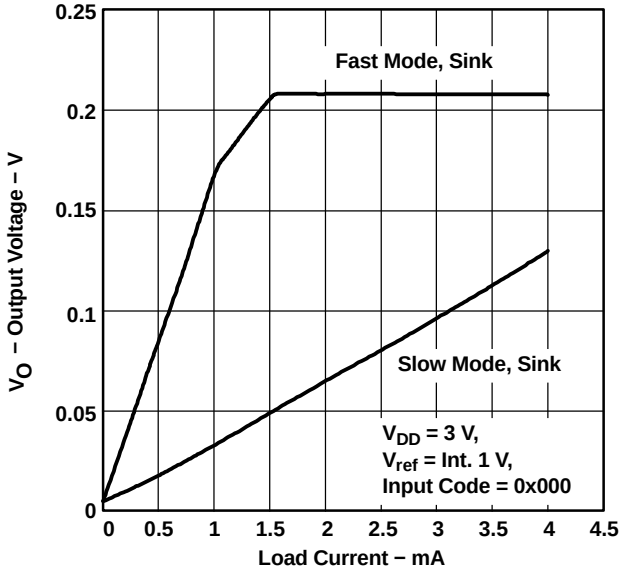


Figure 7.

TYPICAL CHARACTERISTICS (continued)

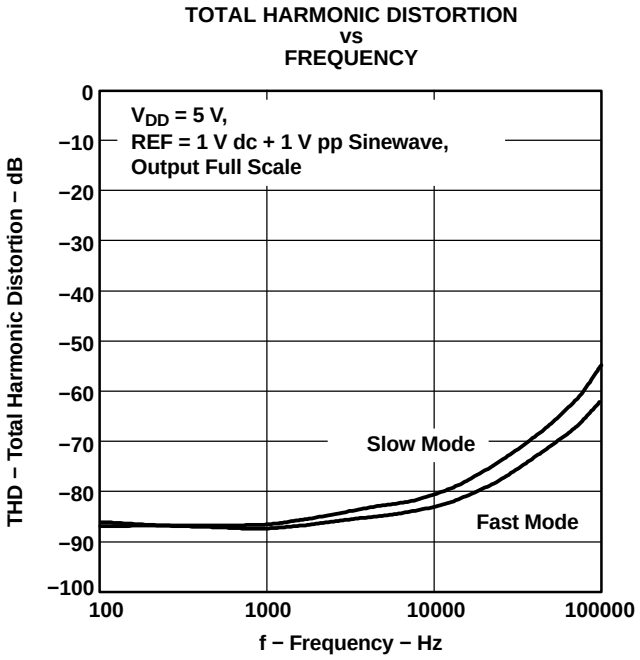


Figure 8.

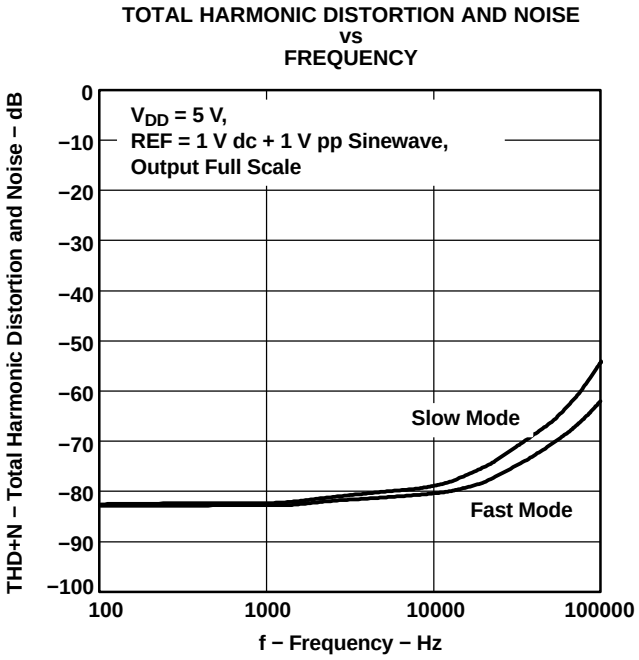


Figure 9.

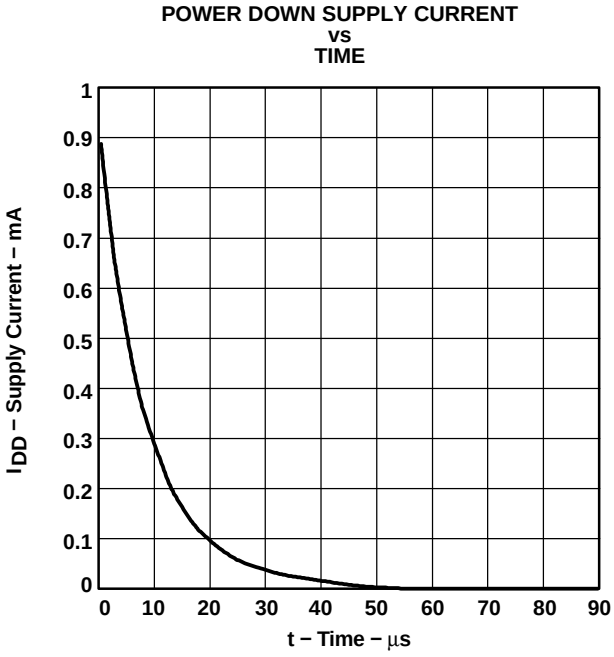


Figure 10.

APPLICATION INFORMATION

GENERAL FUNCTION

The TLV5639 is a 12-bit, single supply DAC, based on a resistor string architecture. It consists of a parallel interface, a speed and power down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer. The output voltage (full scale determined by reference) is given by:

$$2\ \mathrm{REF}\ \frac{\mathrm{CODE}}{0\mathrm{x}1000}\ [\mathrm{V}]$$

Where REF is the reference voltage and CODE is the digital input value in the range 0x000 to 0xFFF. A power-on reset initially puts the internal latches to a defined state (all bits zero).

PARALLEL INTERFACE

The device latches data on the positive edge of $\overline{WE}$. It must be enabled with $\overline{CS}$ low. Whether the data is written to the DAC holding latch or the control register depends on REG. REG = 0 selects the DAC holding latch,REG = 1 selects the control register. $\overline{LDAC}$ low updates the DAC with the value in the holding latch. $\overline{LDAC}$ is an asynchronous input and can be held low, if a separate update is not necessary. However, to control the DAC using the load feature, there should be approximately a 5 ns delay after the positive $\overline{WE}$ edge before driving $\overline{LDAC}$ low.

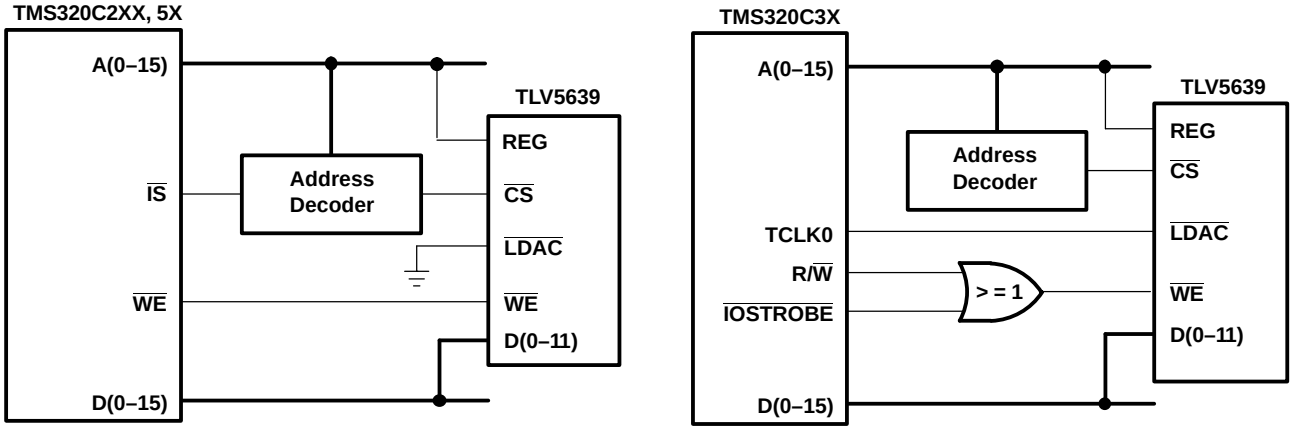


Figure 11.

DATA FORMAT

The TLV5639 writes data either to the DAC holding latch or to the control register, depending on the level of the REG input.

Data destination:

REG = 0 → DAC holding latch

REG = 1 → control register

APPLICATION INFORMATION (continued)

The following table lists the meaning of the bits within the control register:

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	REF1	REF0	X	PWR	SPD
X(1)	X(1)	X(1)	X(1)	X(1)	X(1)	X(1)	0(1)	0(1)	X(1)	0(1)	0(1)

(1) Default values

SPD : Speed control bit 1 = fast mode 0 = slow mode

PWR : Power control bit 1 = power down 0 = normal operation

REF1 and REF0 determine the reference source and the reference voltage.

REFERENCE BITS

REF1	REF0	REFERENCE
0	0	External
0	1	1.024 V
1	0	2.048 V
1	1	External

If an external reference voltage is applied to the REF pin, external reference must be selected.

LINEARITY, OFFSET, AND GAIN ERROR USING SINGLE END SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 12.

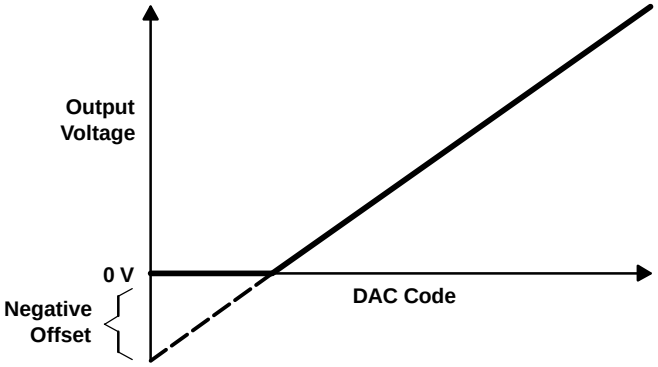


Figure 12. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full scale code and the lowest code that produces a positive output voltage.

TLV5639 INTERFACED to TMS320C203 DSP

HARDWARE INTERFACE

Figure 13 shows an example of the connection between the TLV5639 and the TMS320C203 DSP. The only other device that is needed in addition to the DSP and the DAC is the 74AC138 address decoding circuit . Using this configuration, the DAC data is at address 0x0084 and the DAC control word is at address 0x0085 within the I/O memory space of the TMS320C203.

$\overline{\text{LDAC}}$ is tied low so that the output voltage is updated on the rising $\overline{\text{WE}}$ edge.

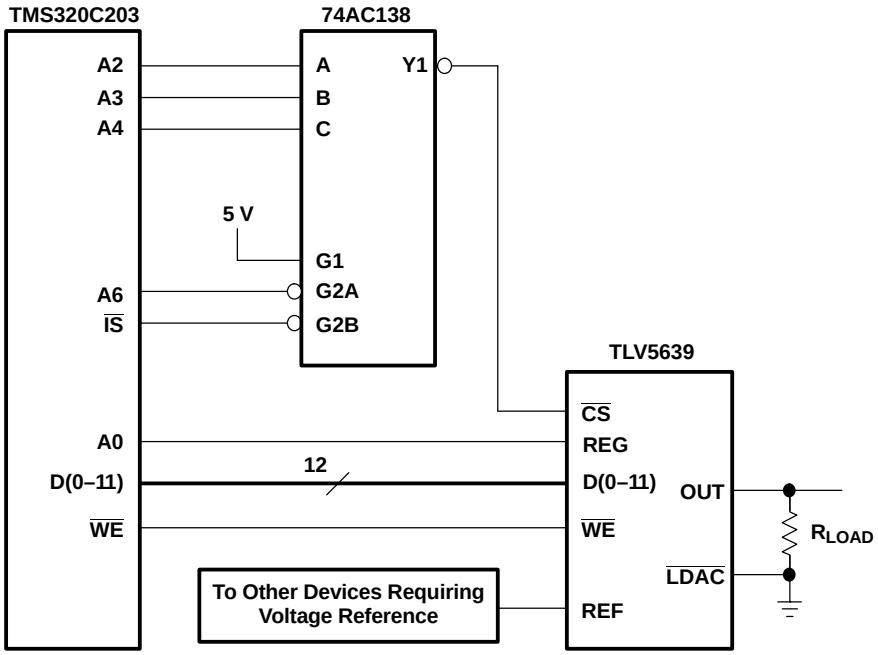


Figure 13. TLV5639 to TMS320C203 DSP Interface Connection

SOFTWARE

Writing data or control information to the TLV5639 is done using a single command. For example, the line of code which reads:

```
out    62h,  dac_ctrl
```

writes the contents of address 0x0062 to the I/O address equated to dac_ctrl (0x0085, the address where the DAC control register has been mapped).

The following code shows how to set the DAC up to use the internal reference and operate in FAST mode by a write to the control register. Timer interrupts are then enabled and repeatedly generated every 205 µs to provide a timebase for synchronizing the waveform generation. In this example, the waveform is generated by simply incrementing a counter and outputting the counter value to the DAC data word once every timer interrupt. This results in a saw waveform.

```
; File:        RAMP.ASM
; Function:    ramp generation with TLV5639
; Processors:  TMS320C203
; { 1999 Texas Instruments


;---------- I/O and memory mapped regs ---------------
     .include regs.asm
dac_data
.equ
0084h
dac_ctrl
.equ
0085h
;------------- vectors -------------------------------
      .ps
0h

b
start
      b
INT1
      b
INT23
      b
TIM_ISR


 ----------Main Program----------
     .ps
1000h
     .entry
start:
     ldp
#0
; set data page to 0
; disable interrupts
     setc
INTM
; disable maskable interrupts
     splk
#0ffffh, IFR
     splk
#0004h,  IMR


; set up the timer
     splk
#0000h,  60h
     splk
#0042h,  61h

out
61h, PRD
     out
60h, TIM

splk
#0c2fh,   62h
     out
62h,   TCR

        splk
#0011h,  62h   ; set up the DAC
; SPD=1  (FAST mode) and ; REF1=1  (2.048 V internal ref enable)
     out
```

```
62h, dac_ctrl


     clrc
INTM
          ; enable interrupts


; loop forever!
next
  idle
b
    next


---------- Interrupt Service Routines----------


INT1:
 ret
; do nothing and return
INT23:
ret
; do nothing and return
TIM_ISR:
; timer interrupt handler
     add
#1h
; increment accumulator

sacl
60h
     out
60h, dac_data  ; write to DAC
     clrc
intm
          ; re-enable interrupts
     ret
              ; return from interrupt
     .END
```

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5639CDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5639C	Samples
TLV5639CPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5639	Samples
TLV5639IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5639I	Samples
TLV5639IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5639	Samples
TLV5639IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5639	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

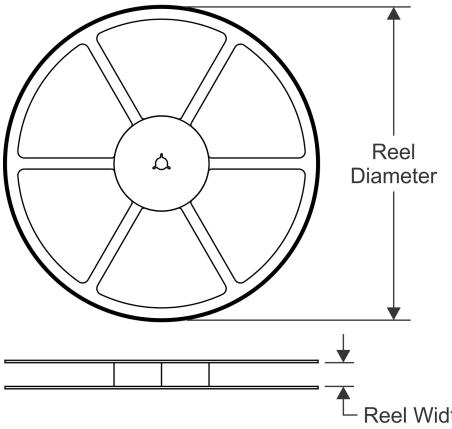
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

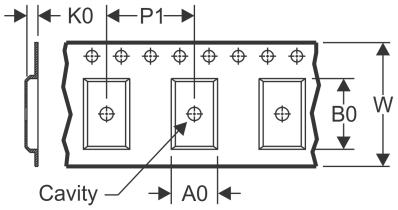
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

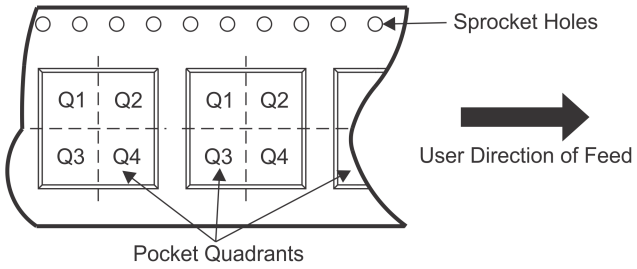


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

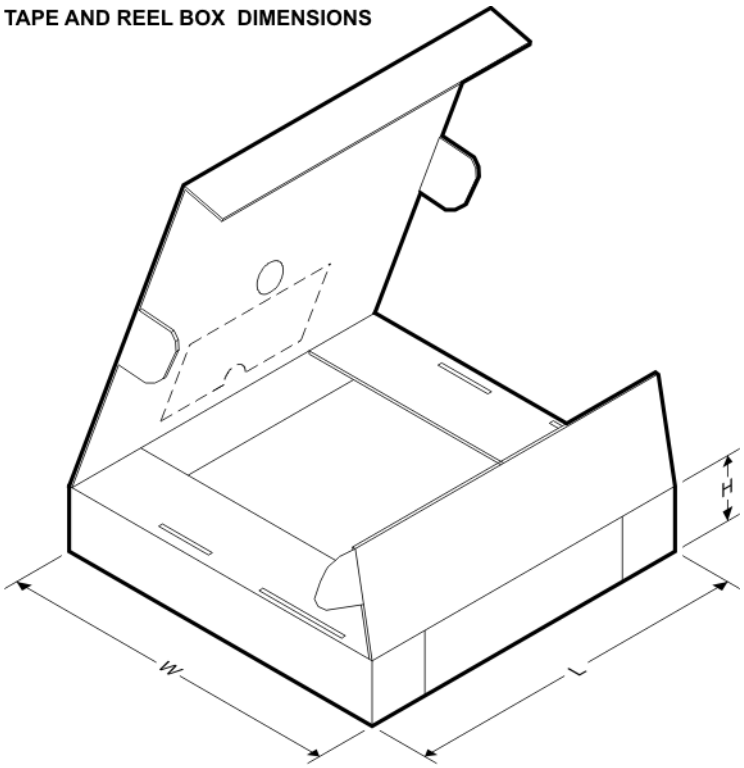
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5639IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

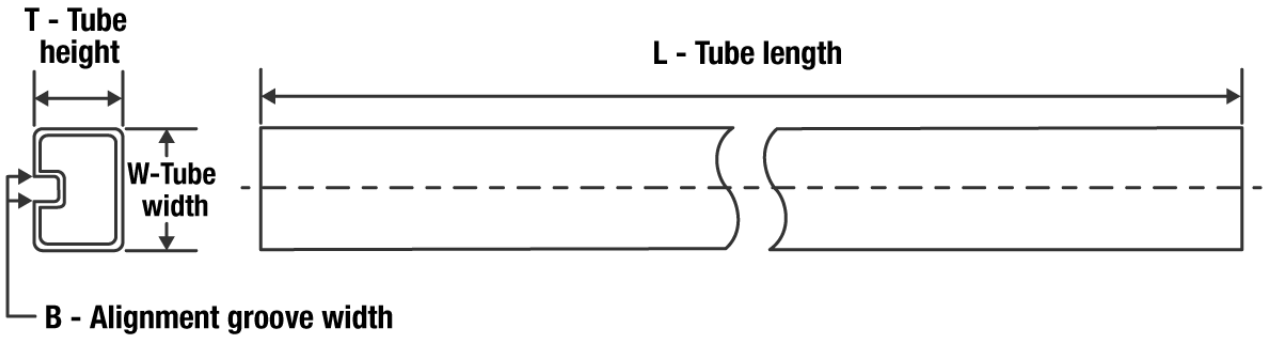
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5639IPWR	TSSOP	PW	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

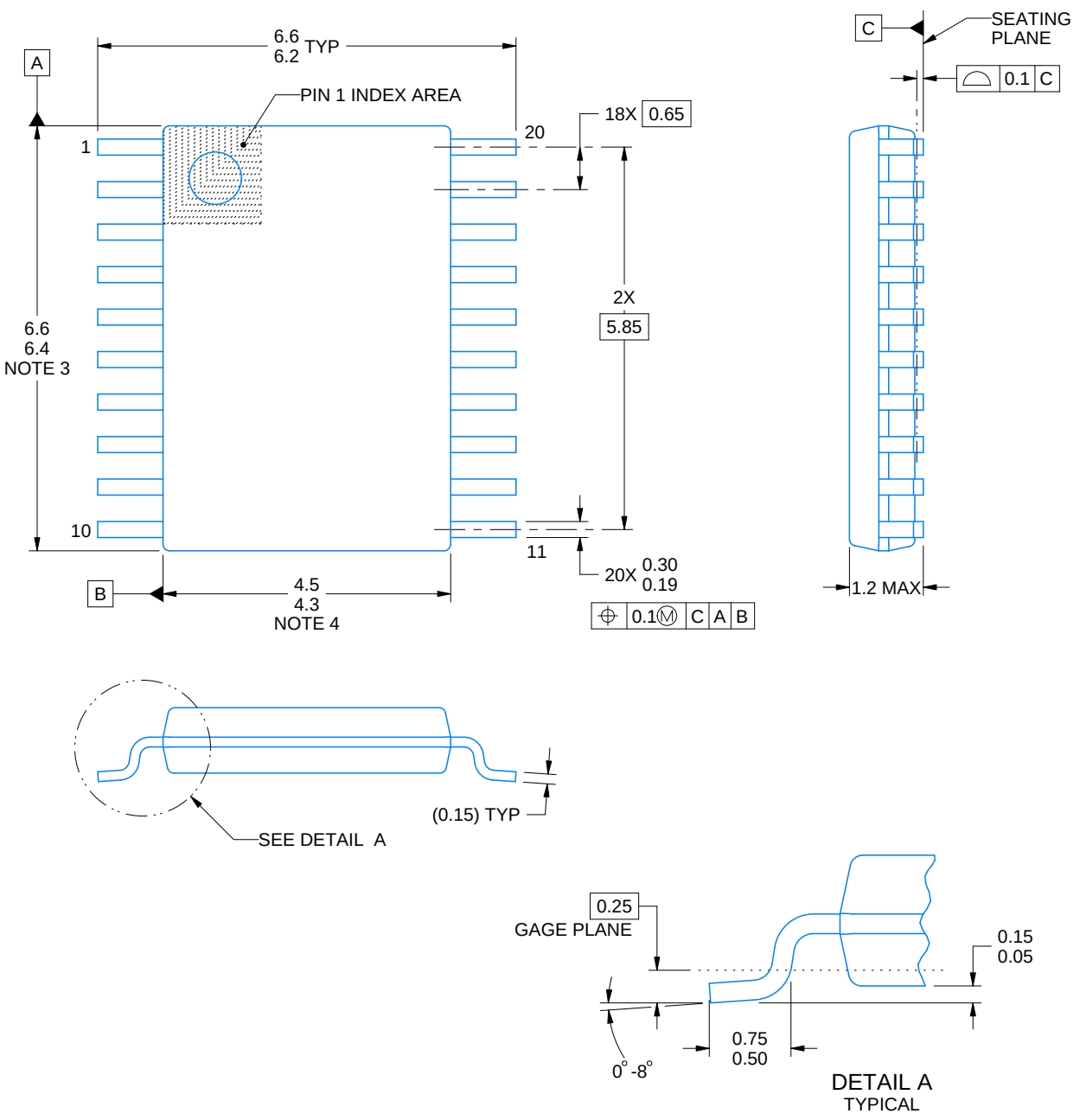
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5639CDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV5639CPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLV5639IDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV5639IPW	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

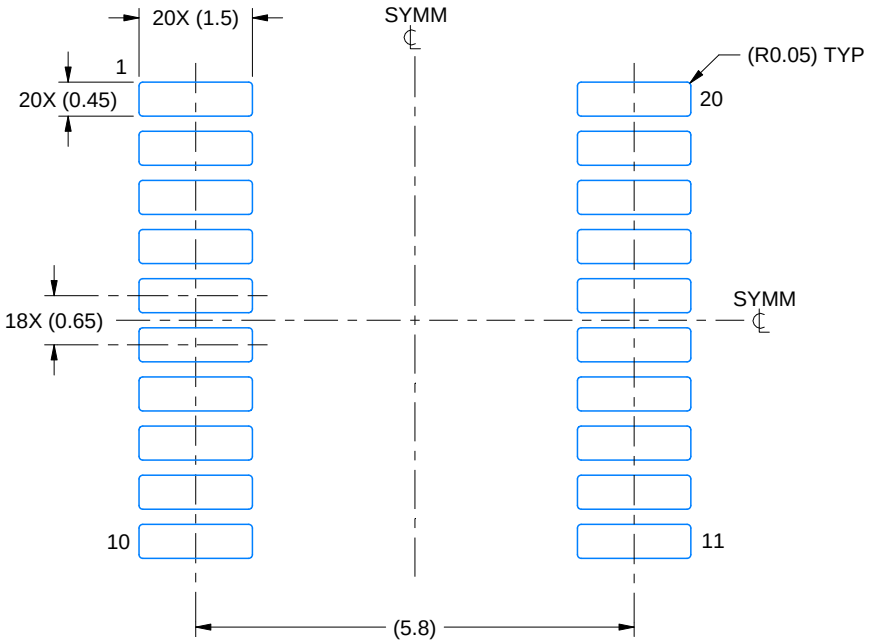
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



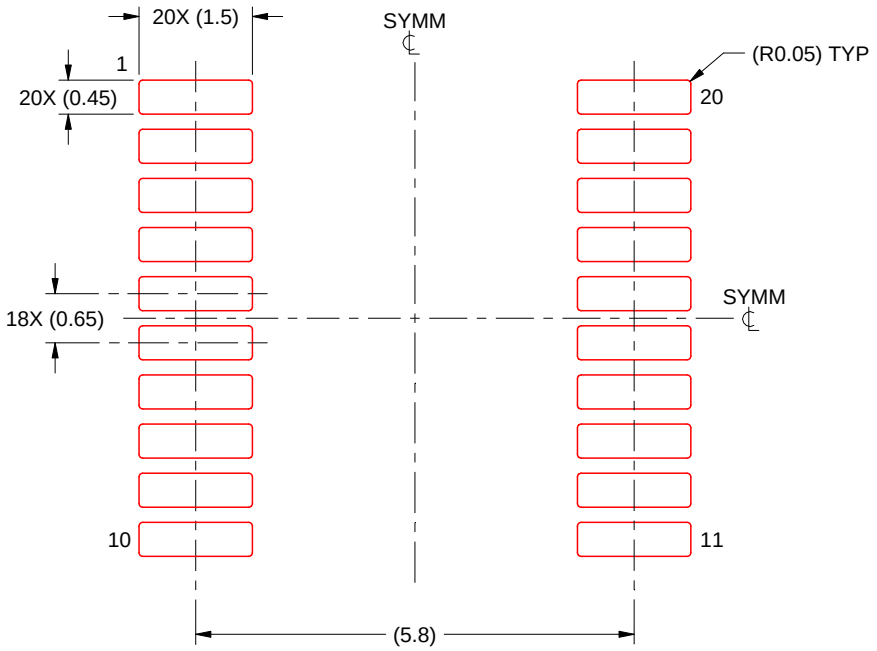
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



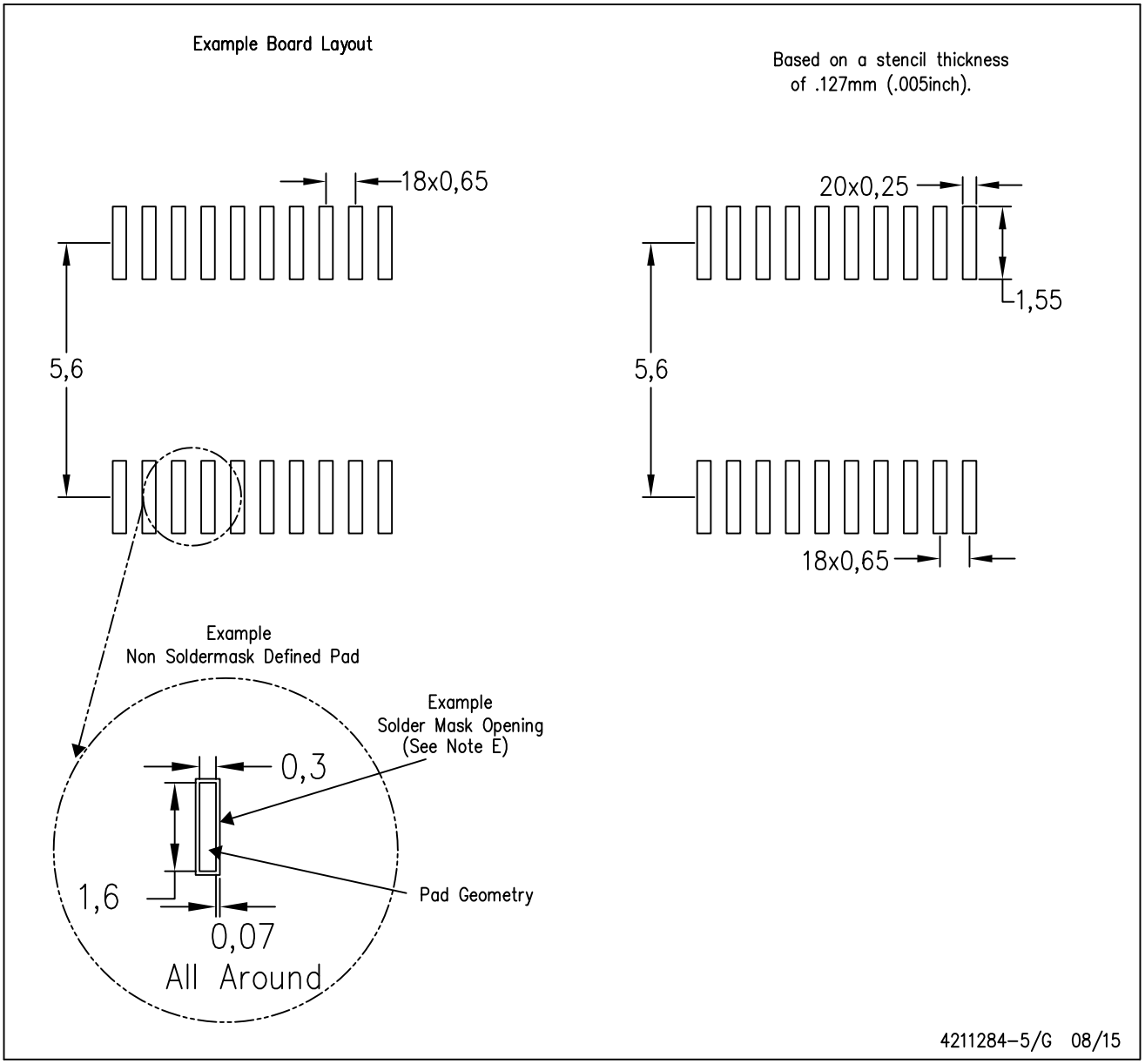
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

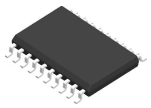
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

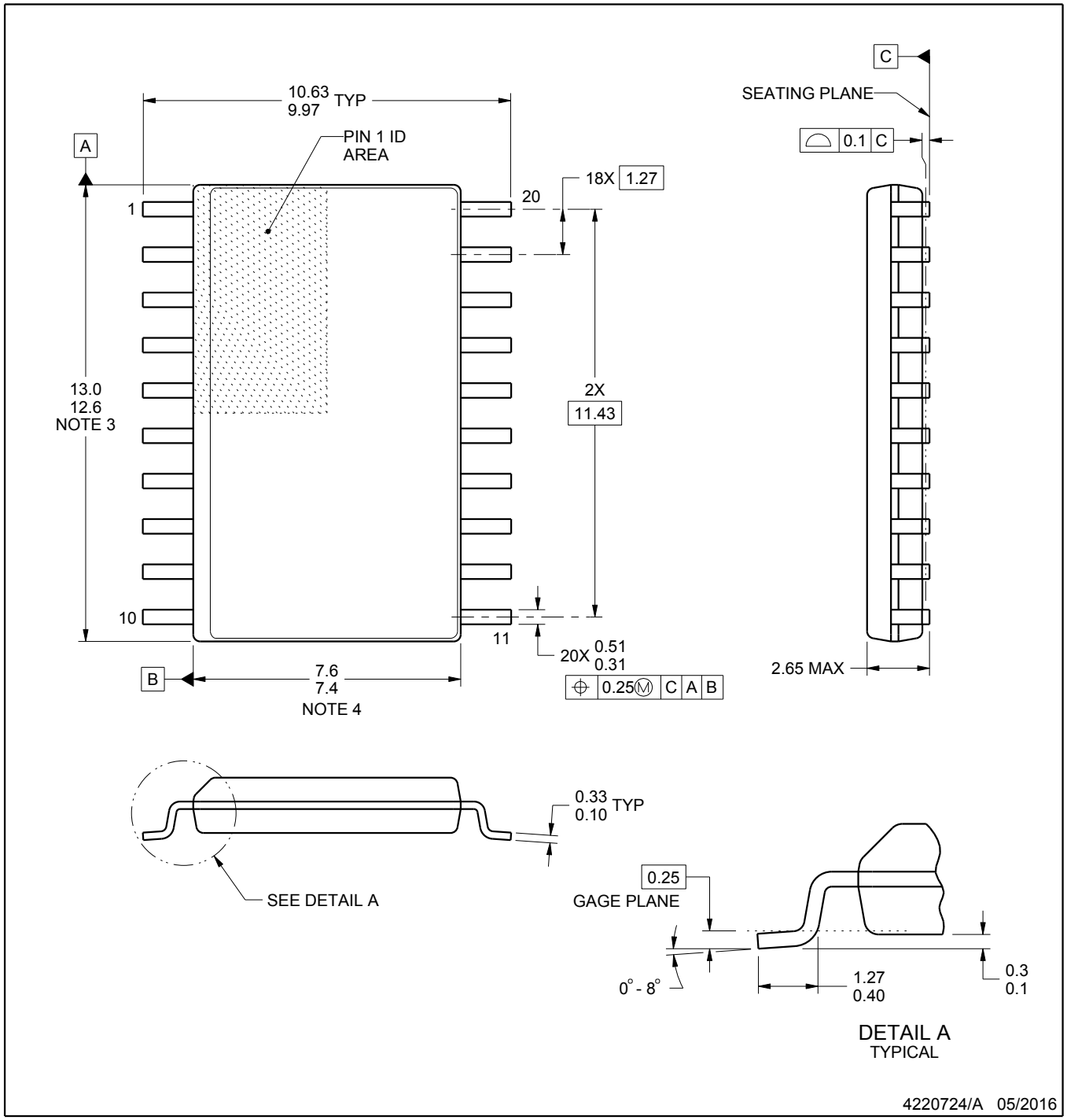


PACKAGE OUTLINE

DW0020A

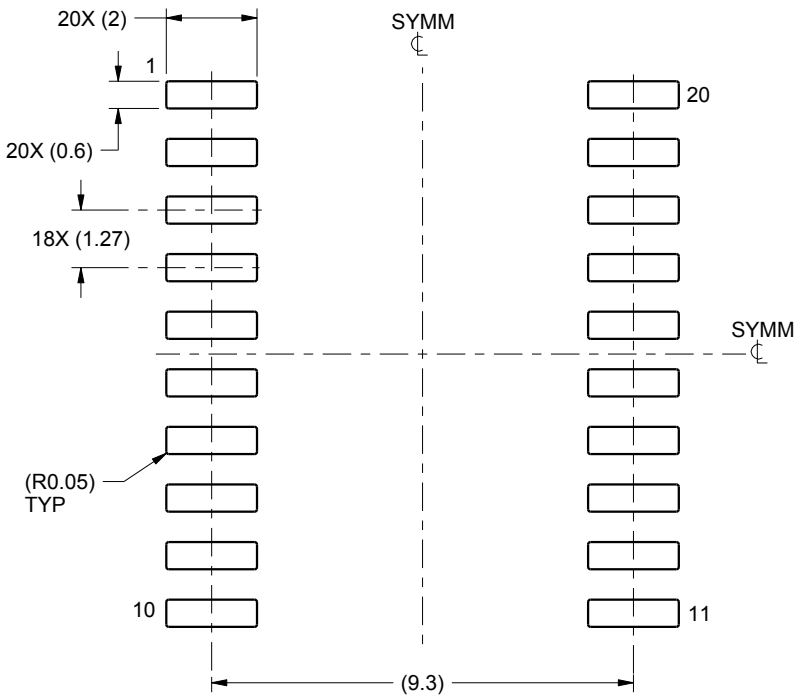
SOIC - 2.65 mm max height

SOIC

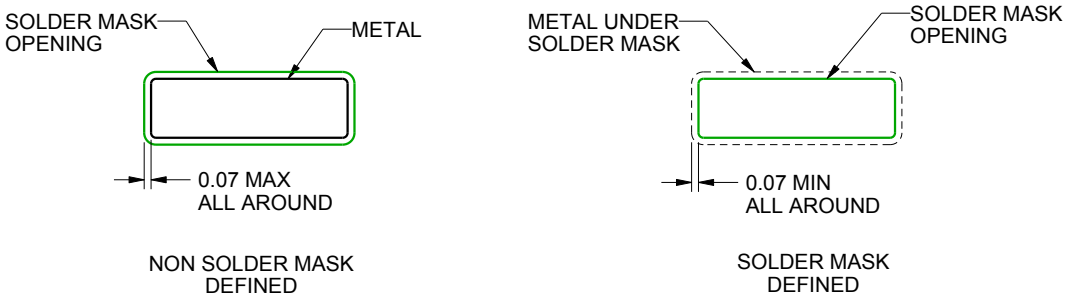


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

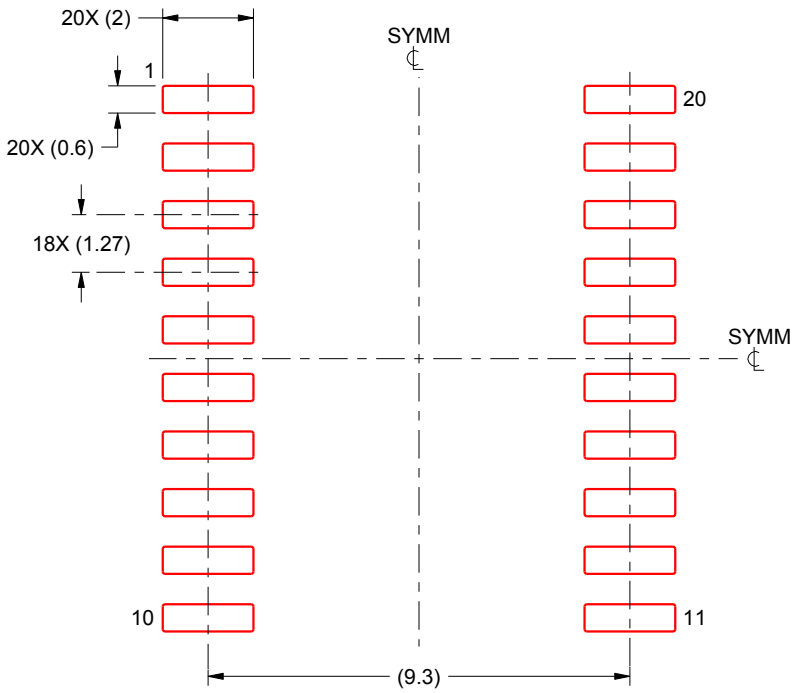


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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