

# LC75810E, LC75810T

## 1/8 to 1/10-Duty Dot Matrix LCD Controller / Driver



ON Semiconductor®

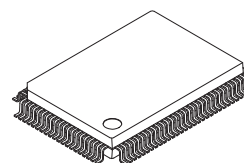
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### Overview

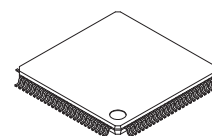
The LC75810E and LC75810T are 1/8 to 1/10 duty dot matrix LCD display controllers/drivers that support the display of characters, numbers, and symbols. In addition to generating dot matrix LCD drive signals based on data transferred serially from a microcontroller, the LC75810E and LC75810T also provide on-chip character display ROM and RAM to allow display systems to be implemented easily.

### Features

- Controls and drives a  $5 \times 7$ ,  $5 \times 8$ , or  $5 \times 9$  dot matrix LCD.
- Supports accessory display segment drive (up to 80 segments)
- Display technique:
  - 1/8-duty, 1/4-bias drive ( $5 \times 7$  dots,  $6 \times 7$  dots)
  - 1/9-duty, 1/4-bias drive ( $5 \times 8$  dots,  $6 \times 8$  dots)
  - 1/10-duty, 1/4-bias drive ( $5 \times 9$  dots,  $6 \times 9$  dots)
- Display digits:
  - 16 digits  $\times$  1 line ( $5 \times 7$  dots),
  - 15 digits  $\times$  1 line ( $5 \times 8$  or  $5 \times 9$  dots)
  - 13 digits  $\times$  1 line ( $6 \times 7$ ,  $6 \times 8$ , or  $6 \times 9$  dots)
- Display control memory
  - CGROM: 240 characters ( $5 \times 7$ ,  $5 \times 8$ , or  $5 \times 9$  dots)
  - CGRAM: 16 characters ( $5 \times 7$ ,  $5 \times 8$ , or  $5 \times 9$  dots)
  - DCRAM:  $64 \times 8$  bits
  - ALATCH: 80 bits
- Instruction function
  - Display on/off control
  - Smooth up, down, left, and right scrolling of the display
- Provides a backup function based on power saving mode
- The frame frequency of the common and segment output waveforms can be controlled by instructions.
- Built-in display contrast adjustment circuit
- Serial data input supports CCB\* format communication with the system controller
- Independent LCD driver block power supply  $V_{LCD}$
- Provides a  $\overline{RES}$  pin for IC internal initialization.
- RC oscillator circuit



PQFP100 14x20 / QIP100E  
[LC75810E]



TQFP100 14x14 / TQIP100  
[LC75810T]

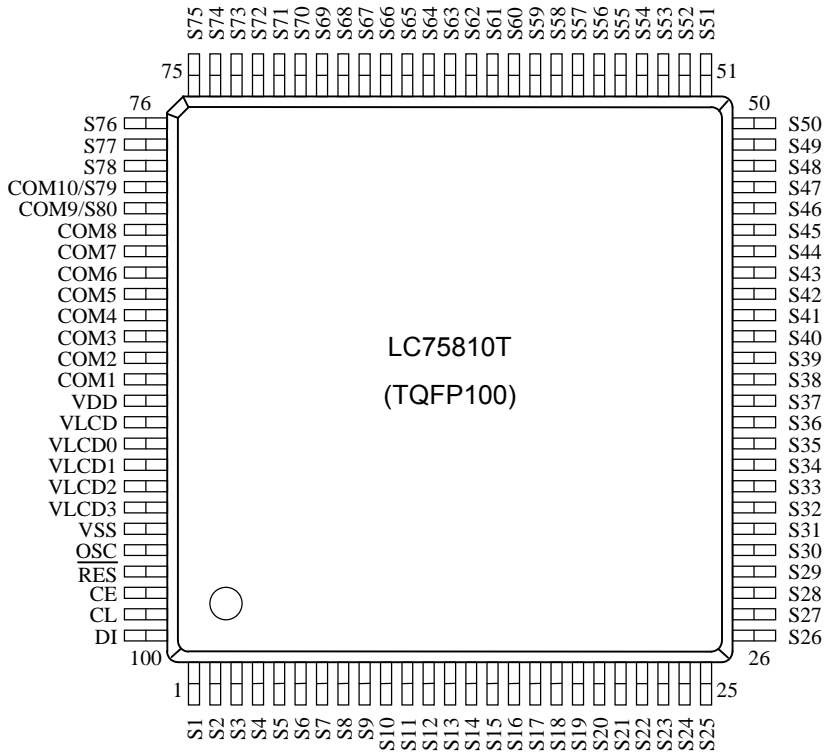
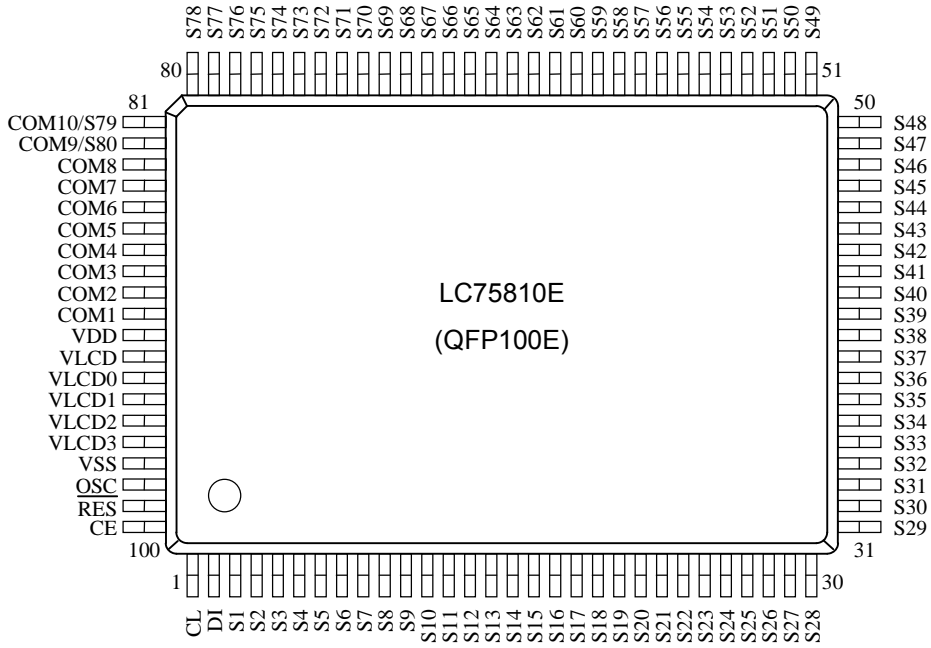
\* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 55 of this data sheet.

# LC75810E, LC75810T

## Pin Assignments (Top view)



# LC75810E, LC75810T

## Specifications

### Absolute Maximum Ratings at Ta = 25°C, V<sub>SS</sub> = 0 V

| Parameter                   | Symbol               | Conditions  | Ratings                        | Unit |
|-----------------------------|----------------------|---|--------------------------------|------|
| Maximum supply voltage      | V <sub>DD max</sub>  | V <sub>DD</sub>   | -0.3 to +7.0                   | V    |
|                             | V <sub>LCD max</sub> | V <sub>LCD</sub>  | -0.3 to +11.0                  |      |
| Input voltage               | V <sub>IN1</sub>     | CE, CL, DI, $\overline{\text{RES}}$                       | -0.3 to +7.0                   | V    |
|                             | V <sub>IN2</sub>     | OSC   | -0.3 to V <sub>DD</sub> + 0.3  |      |
|                             | V <sub>IN3</sub>     | V <sub>LCD1</sub> , V <sub>LCD2</sub> , V <sub>LCD3</sub> | -0.3 to V <sub>LCD</sub> + 0.3 |      |
| Output voltage              | V <sub>OUT1</sub>    | OSC   | -0.3 to V <sub>DD</sub> + 0.3  | V    |
|                             | V <sub>OUT2</sub>    | V <sub>LCD0</sub> , S1 to S80, COM1 to COM10              | -0.3 to V <sub>LCD</sub> + 0.3 |      |
| Output current              | I <sub>OUT1</sub>    | S1 to S80   | 300                            | μA   |
|                             | I <sub>OUT2</sub>    | COM1 to COM10   | 3                              | mA   |
| Allowable power dissipation | Pd max               | Ta = 85°C   | 200                            | mW   |
| Operating temperature       | Topr                 |   | -40 to +85                     | °C   |
| Storage temperature         | Tstg                 |   | -55 to +125                    | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### Allowable Operating Ranges at Ta = -40 to +85°C, V<sub>SS</sub> = 0 V

| Parameter                        | Symbol            | Conditions  | Ratings             |                       |                     | Unit |
|----------------------------------|-------------------|---|---------------------|-----------------------|---------------------|------|
|                                  |                   |   | min.                | typ.                  | max.                |      |
| Supply voltage                   | V <sub>DD</sub>   | V <sub>DD</sub>   | 2.7                 |                       | 6.0                 | V    |
|                                  | V <sub>LCD</sub>  | When the display contrast adjustment circuit is used.     | 7.0                 |                       | 10.0                |      |
|                                  |                   | When the display contrast adjustment circuit is not used. | 4.5                 |                       | 10.0                |      |
| Output voltage                   | V <sub>LCD0</sub> | V <sub>LCD0</sub>   | 4.5                 |                       | V <sub>LCD</sub>    | V    |
| Input voltage                    | V <sub>LCD1</sub> | V <sub>LCD1</sub>   |                     | 3/4 V <sub>LCD0</sub> | V <sub>LCD0</sub>   | V    |
|                                  | V <sub>LCD2</sub> | V <sub>LCD2</sub>   |                     | 2/4 V <sub>LCD0</sub> | V <sub>LCD0</sub>   |      |
|                                  | V <sub>LCD3</sub> | V <sub>LCD3</sub>   |                     | 1/4 V <sub>LCD0</sub> | V <sub>LCD0</sub>   |      |
| Input high level voltage         | V <sub>IH</sub>   | CE, CL, DI, $\overline{\text{RES}}$                       | 0.8 V <sub>DD</sub> |                       | 6.0                 | V    |
| Input low level voltage          | V <sub>IL</sub>   | CE, CL, DI, $\overline{\text{RES}}$                       | 0                   |                       | 0.2 V <sub>DD</sub> | V    |
| Recommended external resistance  | Rosc              | OSC   |                     | 10                    |                     | kΩ   |
| Recommended external capacitance | Cosc              | OSC   |                     | 470                   |                     | pF   |
| Guaranteed oscillation range     | fosc              | OSC   | 150                 | 300                   | 600                 | kHz  |
| Data setup time                  | tds               | CL, DI (Figure 2)   | 160                 |                       |                     | ns   |
| Data hold time                   | tdh               | CL, DI (Figure 2)   | 160                 |                       |                     | ns   |
| CE wait time                     | tcp               | CE, CL (Figure 2)   | 160                 |                       |                     | ns   |
| CE setup time                    | tcs               | CE, CL (Figure 2)   | 160                 |                       |                     | ns   |
| CE hold time                     | tch               | CE, CL (Figure 2)   | 160                 |                       |                     | ns   |
| High level clock pulse width     | tφH               | CL (Figure 2)   | 160                 |                       |                     | ns   |
| Low level clock pulse width      | tφL               | CL (Figure 2)   | 160                 |                       |                     | ns   |
| Minimum reset pulse width        | tWRES             | $\overline{\text{RES}}$ (Figure 3)                        | 1                   |                       |                     | μs   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# LC75810E, LC75810T

## Electrical Characteristics for the Allowable Operating Ranges

| Parameter                      | Symbol     | Conditions   | Ratings              |              |                      | Unit    |
|--------------------------------|------------|--|----------------------|--------------|----------------------|---------|
|                                |            |  | min.                 | typ.         | max.                 |         |
| Hysteresis                     | $V_H$      | CE, CL, DI, $\overline{RES}$   |                      | 0.1 $V_{DD}$ |                      | V       |
| Input high level current       | $I_{IH}$   | CE, CL, DI, $\overline{RES}$ : $V_i = 6.0$ V   |                      |              | 5.0                  | $\mu$ A |
| Input low level current        | $I_{IL}$   | CE, CL, DI, $\overline{RES}$ : $V_i = 0$ V   | -5.0                 |              |                      | $\mu$ A |
| Output high level voltage      | $V_{OH1}$  | S1 to S80: $I_o = -20$ $\mu$ A   | $V_{LCD0} - 0.6$     |              |                      | V       |
|                                | $V_{OH2}$  | COM1 to COM10: $I_o = -100$ $\mu$ A  | $V_{LCD0} - 0.6$     |              |                      |         |
| Output low level voltage       | $V_{OL1}$  | S1 to S80: $I_o = 20$ $\mu$ A  |                      |              | 0.6                  | V       |
|                                | $V_{OL2}$  | COM1 to COM10: $I_o = 100$ $\mu$ A   |                      |              | 0.6                  |         |
| Output middle level voltage *1 | $V_{MID1}$ | S1 to S80: $I_o = \pm 20$ $\mu$ A  | $2/4 V_{LCD0} - 0.6$ |              | $2/4 V_{LCD0} + 0.6$ | V       |
|                                | $V_{MID2}$ | COM1 to COM10: $I_o = \pm 100$ $\mu$ A   | $3/4 V_{LCD0} - 0.6$ |              | $3/4 V_{LCD0} + 0.6$ |         |
|                                | $V_{MID3}$ | COM1 to COM10: $I_o = \pm 100$ $\mu$ A   | $1/4 V_{LCD0} - 0.6$ |              | $1/4 V_{LCD0} + 0.6$ |         |
| Oscillator frequency           | $f_{osc}$  | OSC: $R_{OSC} = 10$ k $\Omega$<br>$C_{OSC} = 470$ pF   | 210                  | 300          | 390                  | kHz     |
| Current drain                  | $I_{DD1}$  | $V_{DD}$ : Power saving mode   |                      |              | 5                    | $\mu$ A |
|                                | $I_{DD2}$  | $V_{DD} = 6.0$ V<br>Output open<br>$f_{osc} = 300$ kHz   |                      | 700          | 1400                 |         |
|                                | $I_{LCD1}$ | $V_{LCD}$ : Power saving mode  |                      |              | 5                    |         |
|                                | $I_{LCD2}$ | $V_{LCD} = 10.0$ V<br>Output open<br>$f_{osc} = 300$ kHz<br>When the display contrast adjustment circuit is used     |                      | 450          | 900                  |         |
|                                | $I_{LCD3}$ | $V_{LCD} = 10.0$ V<br>Output open<br>$f_{osc} = 300$ kHz<br>When the display contrast adjustment circuit is not used |                      | 200          | 400                  |         |

Note \*1: Excluding the bias voltage generation divider resistors built into the  $V_{LCD0}$ ,  $V_{LCD1}$ ,  $V_{LCD2}$ ,  $V_{LCD3}$ , and  $V_{SS}$  pins. (See figure 1.)

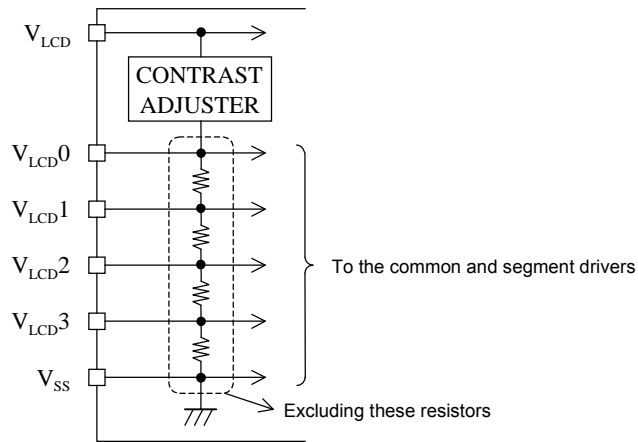
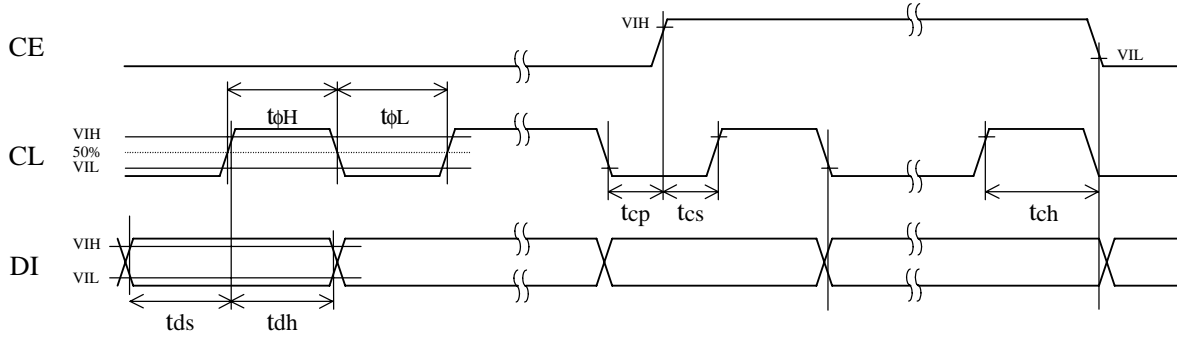


Figure 1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- When CL is stopped at the low level



- When CL is stopped at the high level

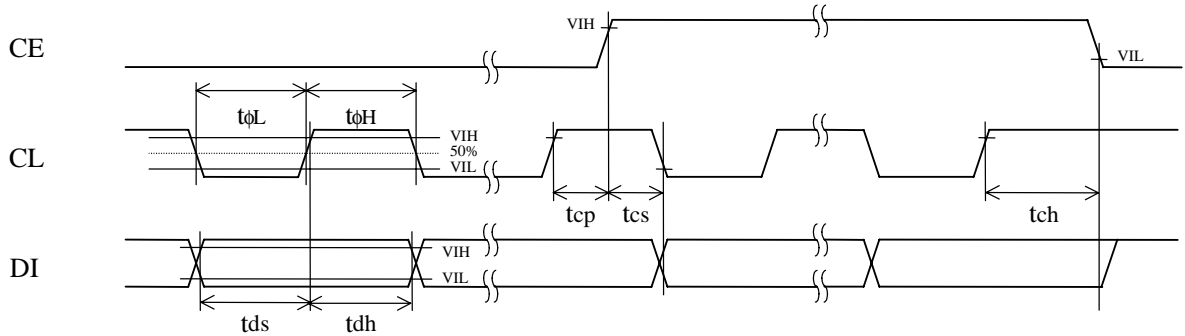
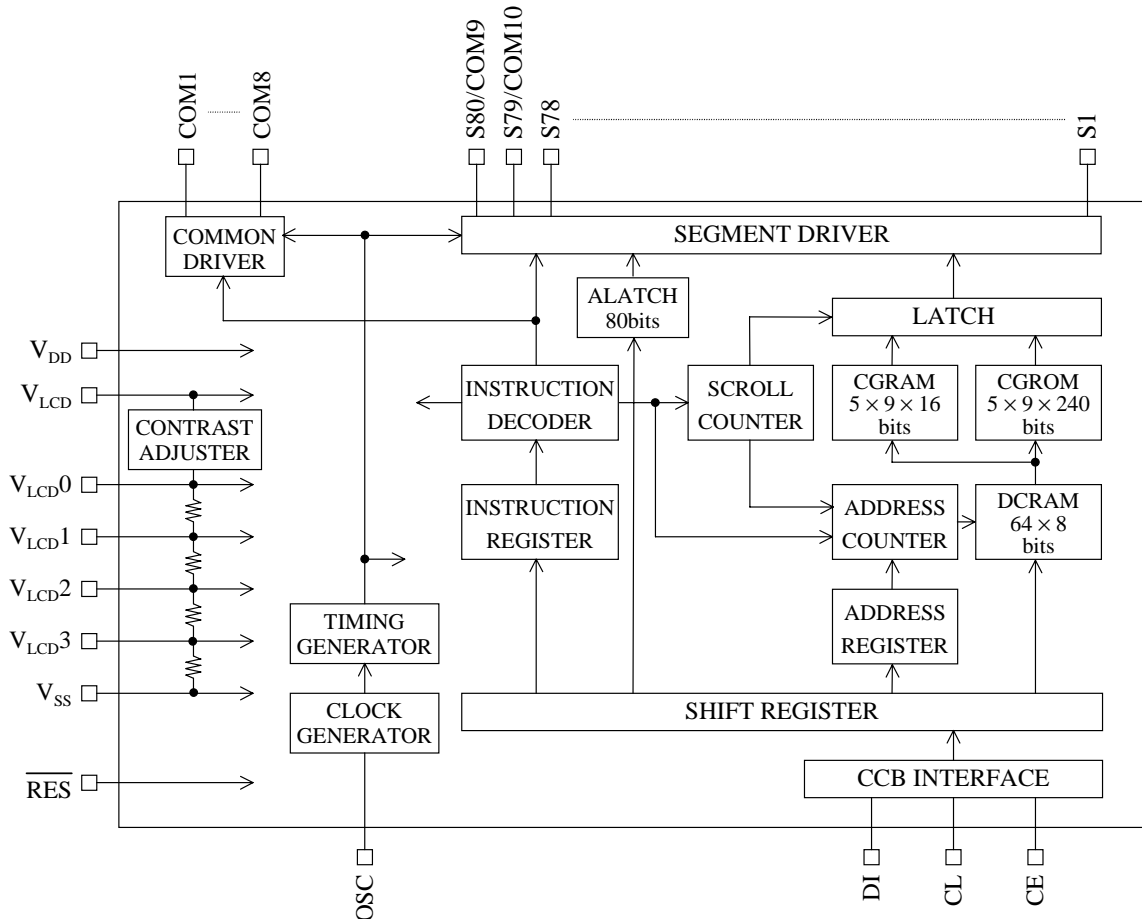



Figure 2

Block Diagram



## LC75810E/T

### Pin Functions

| Pin                                | Pin No.             |                     | Function   | Active level  | I/O | Handling when unused |
|------------------------------------|---------------------|---------------------|--|---|-----|----------------------|
|                                    | LC75810E            | LC75810T            |  |   |     |                      |
| S1 to S78<br>S79/COM10<br>S80/COM9 | 3 to 80<br>81<br>82 | 1 to 78<br>79<br>80 | Segment driver outputs<br>The S79/COM10 and S80/COM9 pins can be used as common driver outputs under the "set display technique" instruction.  | –   | O   | OPEN                 |
| COM1 to COM8                       | 90 to 83            | 88 to 81            | Common driver outputs  | –   | O   | OPEN                 |
| OSC                                | 98                  | 96                  | Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.   | –   | I/O | VDD                  |
| CE                                 | 100                 | 98                  | Serial data transfer inputs. These pins are connected to the microcontroller.<br>CE: Chip enable<br>CL: Synchronization clock<br>DI: Transfer data   | H   | I   | GND                  |
| CL                                 | 1                   | 99                  |  |  | I   |                      |
| DI                                 | 2                   | 100                 |  | –   | I   |                      |
| $\overline{\text{RES}}$            | 99                  | 97                  | Reset signal input<br><ul style="list-style-type: none"> <li>• When <math>\overline{\text{RES}}</math> is low (<math>V_{SS}</math>) <ul style="list-style-type: none"> <li>– Display off</li> <li>S1 to S78 = "L" (<math>V_{SS}</math>)</li> <li>S79/COM10 and S80/COM9 = "L" (<math>V_{SS}</math>)</li> <li>COM1 to COM8 = "L" (<math>V_{SS}</math>)</li> </ul> </li> <li>– Serial data transfer is disabled.</li> <li>– The OSC pin oscillator is stopped.</li> </ul> <ul style="list-style-type: none"> <li>• When <math>\overline{\text{RES}}</math> is high (<math>V_{DD}</math>) <ul style="list-style-type: none"> <li>– Display on after a "display on/off control" (display on state setting) instruction is executed.</li> <li>– Serial data transfers are enabled.</li> <li>– The OSC pin oscillator operates.</li> </ul> </li> </ul> | L   | I   | GND                  |
| $V_{LCD0}$                         | 93                  | 91                  | LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, $V_{LCD0}$ must be greater than or equal to 4.5 V. Also, external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.  | –   | O   | OPEN                 |
| $V_{LCD1}$                         | 94                  | 92                  | LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 $V_{LCD0}$ voltage level externally.  | –   | I   | OPEN                 |
| $V_{LCD2}$                         | 95                  | 93                  | LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 $V_{LCD0}$ voltage level externally.  | –   | I   | OPEN                 |
| $V_{LCD3}$                         | 96                  | 94                  | LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 $V_{LCD0}$ voltage level externally.  | –   | I   | OPEN                 |
| $V_{DD}$                           | 91                  | 89                  | Logic block power supply connection. Provide a voltage of between 2.7 and 6.0 V.   | –   | –   | –                    |
| $V_{LCD}$                          | 92                  | 90                  | LCD driver block power supply connection. Provide a voltage of between 7.0 and 10.0 V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 and 10.0 V when the circuit is not used.   | –   | –   | –                    |
| $V_{SS}$                           | 97                  | 95                  | Power supply connection. Connect to ground.  | –   | –   | –                    |

**Block Functions**

• AC (Address counter)

AC is a counter that provides the DCRAM address.

The address is automatically modified internally, and the LCD display state is retained.

• DCRAM (Data control RAM)

DCRAM is the RAM that is used to store display data expressed as 8-bit character codes. (These character codes are converted to  $5 \times 7$ ,  $5 \times 8$ , or  $5 \times 9$  dot matrix character patterns using CGROM or CGRAM.)

DCRAM has a capacity of  $64 \times 8$  bits, and can hold 64 characters. The table below lists the correspondence between the 6-bit DCRAM address loaded into AC and the display position on the LCD panel.

- For a  $64 \text{ digits} \times 1 \text{ line}$  display structure (For a “set display technique” instruction with  $0Z1 = 0$  and  $0Z2 = 0$ )  
When the DCRAM address loaded into AC is 00H

| Display digit                  |            | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |  | 61 | 62 | 63 | 64 |
|--------------------------------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|----|----|----|----|
| DCRAM address<br>(hexadecimal) | First line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 |  | 3C | 3D | 3E | 3F |

However, when the display smooth scrolling is performed, the DCRAM address shifts as follows.

| Display digit                  |            | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |  | 61 | 62 | 63 | 64 |
|--------------------------------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|----|----|----|----|
| DCRAM address<br>(hexadecimal) | First line | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 |  | 3D | 3E | 3F | 00 |

Shift to the left by 1 character digit

| Display digit                  |            | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |  | 61 | 62 | 63 | 64 |
|--------------------------------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|----|----|----|----|
| DCRAM address<br>(hexadecimal) | First line | 3F | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 |  | 3B | 3C | 3D | 3E |

Shift to the right by 1 character digit

Note that the display area on the LCD is display digits 1 to 16 on the first line when a display technique is  $5 \times 7$ ,  $5 \times 8$ , or  $5 \times 9$  dots, and it is display digits 1 to 13 on the first line when a display technique is  $6 \times 7$ ,  $6 \times 8$ , or  $6 \times 9$  dots.

- For a  $32 \text{ digits} \times 2 \text{ lines}$  display structure (For a “set display technique” instruction with  $0Z1 = 1$  and  $0Z2 = 0$ )  
When the DCRAM address loaded into AC is 00H

| Display digit                  |             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |  | 29 | 30 | 31 | 32 |
|--------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|----|----|----|----|
| DCRAM address<br>(hexadecimal) | First line  | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 |  | 1C | 1D | 1E | 1F |
|                                | Second line | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F | 30 | 31 |  | 3C | 3D | 3E | 3F |

However, when the display smooth scrolling is performed, the DCRAM address shifts as follows.

| Display digit                  |             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |  | 29 | 30 | 31 | 32 |
|--------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|----|----|----|----|
| DCRAM address<br>(hexadecimal) | First line  | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 |  | 1D | 1E | 1F | 00 |
|                                | Second line | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F | 30 | 31 | 32 |  | 3D | 3E | 3F | 20 |

Shift to the left by 1 character digit

| Display digit                  |             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |  | 29 | 30 | 31 | 32 |
|--------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|----|----|----|----|
| DCRAM address<br>(hexadecimal) | First line  | 1F | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 |  | 1B | 1C | 1D | 1E |
|                                | Second line | 3F | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F | 30 |  | 3B | 3C | 3D | 3E |

Shift to the right by 1 character digit

| Display digit                  |             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |  | 29 | 30 | 31 | 32 |
|--------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|----|----|----|----|
| DCRAM address<br>(hexadecimal) | First line  | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F | 30 | 31 |  | 3C | 3D | 3E | 3F |
|                                | Second line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 |  | 1C | 1D | 1E | 1F |

Shift to the up or down by 1 character digit

Note that the display area on the LCD is display digits 1 to 16 on the first line when a display technique is  $5 \times 7$ ,  $5 \times 8$ , or  $5 \times 9$  dots, and it is display digits 1 to 13 on the first line when a display technique is  $6 \times 7$ ,  $6 \times 8$ , or  $6 \times 9$  dots.

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- For a 16 digits × 4 lines display structure (For a “set display technique” instruction with 0Z1 = 0 and 0Z2 = 1)  
When the DCRAM address loaded into AC is 00H

| Display digit               | 1           | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |    |
|-----------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DCRAM address (hexadecimal) | First line  | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
|                             | Second line | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
|                             | Third line  | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
|                             | Fourth line | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |

However, when the display smooth scrolling is performed, the DCRAM address shifts as follows.

| Display digit               | 1           | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |    |
|-----------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DCRAM address (hexadecimal) | First line  | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 00 |
|                             | Second line | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 |
|                             | Third line  | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F | 20 |
|                             | Fourth line | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F | 30 |

Shift to the left by 1 character digit

| Display digit               | 1           | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |    |
|-----------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DCRAM address (hexadecimal) | First line  | 0F | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E |
|                             | Second line | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E |
|                             | Third line  | 2F | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E |
|                             | Fourth line | 3F | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E |

Shift to the right by 1 character digit

| Display digit               | 1           | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |    |
|-----------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DCRAM address (hexadecimal) | First line  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
|                             | Second line | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
|                             | Third line  | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
|                             | Fourth line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |

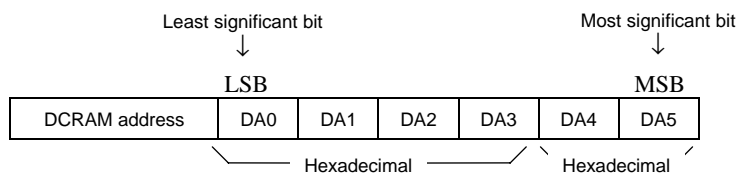
Shift to the up by 1 character digit

| Display digit               | 1           | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |    |
|-----------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DCRAM address (hexadecimal) | First line  | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
|                             | Second line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
|                             | Third line  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
|                             | Fourth line | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |

Shift to the down by 1 character digit

Note that the display area on the LCD is display digits 1 to 16 on the first line when a display technique is 5 × 7, 5 × 8, or 5 × 9 dots, and it is display digits 1 to 13 on the first line when a display technique is 6 × 7, 6 × 8, or 6 × 9 dots.

Note \*2: The DCRAM address is expressed in hexadecimal.



Example: When the DCRAM address is 2EH

|     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|
| DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
| 0   | 1   | 1   | 1   | 0   | 1   |

- Note \*3:
- |            |                      |             |
|------------|----------------------|-------------|
| 5 × 7 dots | ... 16-digit display | 5 × 7 dots. |
| 5 × 8 dots | ... 16-digit display | 4 × 8 dots. |
| 5 × 9 dots | ... 16-digit display | 3 × 9 dots. |
| 6 × 7 dots | ... 13-digit display | 6 × 7 dots. |
| 6 × 8 dots | ... 13-digit display | 6 × 8 dots. |
| 6 × 9 dots | ... 13-digit display | 6 × 9 dots. |



- CGROM (Character generator ROM)  
CGROM is the ROM that is used to generate the 240 kinds of 5 × 7, 5 × 8, or 5 × 9 dot matrix character patterns from the 8-bit character codes. CGROM has a capacity of 240 × 45 bits. When a character code is written to DCRAM, the character pattern stored in the CGROM corresponding to the character code is displayed at the position on the LCD corresponding to the DCRAM address loaded into AC.
- CGRAM (Character generator RAM)  
CGRAM is the RAM to which user programs can freely write arbitrary character patterns. Up to 16 kinds of 5 × 7, 5 × 8, or 5 × 9 dot matrix character patterns can be stored. CGRAM has a capacity of 16 × 45 bits.
- ALATCH (Additional data latch)  
ALATCH is the latch that is used to store the ADATA display data for the accessory display. ALATCH has a capacity of 80 bits, and the stored display data is displayed directly without the use of CGROM or CGRAM.
- SC (Scroll counter)  
SC is the counter that is used to scroll the display in the left, right, up, or down directions in dot units. Since this function scrolls in dot units, it implements smooth scrolling.

**Reset Function**

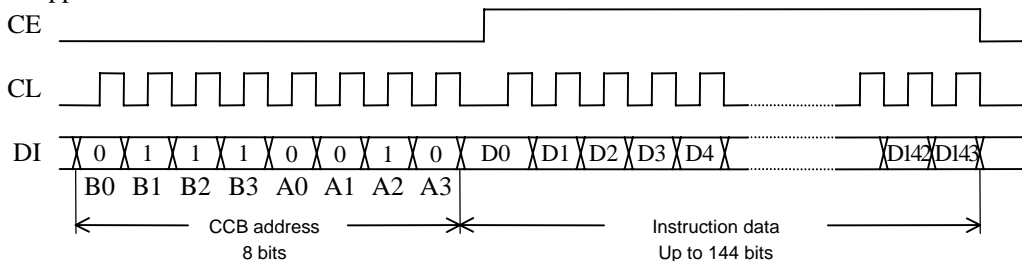
The LC75810E and LC75810T are reset when a low level is applied to the  $\overline{\text{RES}}$  pin at power on and, in normal mode. On a reset the LC75810E and LC75810T create a display with all LCD panels turned off. However, after a reset applications must set the contents of DCRAM, ALATCH, and CGRAM before turning on display with a “display on/off control” instruction since the contents of these memories are undefined. That is, applications must execute the following instructions.

- Set display technique
- DCRAM data write
- ALATCH data write (If ALATCH is used.)
- CGRAM data write (IF CGRAM is used.)
- Set AC and SC addresses
- Set display contrast (If the display contrast adjustment circuit is used.)

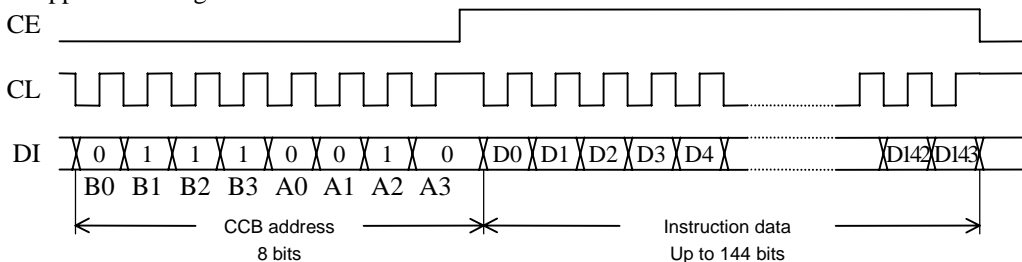
After executing the above instructions, applications must turn on the display with a “display on/off control” instruction. Note that when applications turn off in the normal mode, applications must turn off the display with a “display on/off control” instruction. (See the detailed instruction descriptions.)

**Serial Data Transfer Format**

- When CL is stopped at the low level



- When CL is stopped at the high level



- CCB address: 4EH
- D0 to D143: Instruction data  
The data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When transferring instruction data from the microcontroller, applications must assure that the time from the transfer of one set of instruction data until the next instruction data transfer is significantly longer than the instruction execution time.

Instruction Table

| Instruction             | D0 D1 ... D55 | D56 D57 ... D79 | D80 D81 ... D111 | D112 D113 D114 D115 D116 D117 D118 D119                  | D120 D121 D122 D123 D124 D125 D126 D127      | D128 D129 D130 D131 D132 D133 D134 D135     | D136 D137 D138 D139  | D140 D141 D142 D143 | Execution time (*4) |
|-------------------------|---------------|-----------------|------------------|--|--|---|----------------------|---------------------|---------------------|
| Set display technique   |               |                 |                  |  |  | OZ1 OZ2 DW X X X X X X X X X X              | DT1 DT2 FC 0 0 0 0 1 |                     | 0 μs                |
| Display on/off control  |               |                 |                  |  | DG1 DG2 DG3 DG4 DG5 DG6 DG7 DG8              | DG9 DG10 DG11 DG12 DG13 DG14 DG15 DG16      | M A SC BU            | 0 0 1 0             | 0 μs/27 μs (*5)     |
| Display scroll          |               |                 |                  |  | HS0 HS1 HS2 X X X X X X X X X X              | VS0 VS1 VS2 VS3 X X X X X X X X X X         | R/L DU X 0 0 0 1 1   |                     | 27 μs/162 μs (*6)   |
| Set AC and SC addresses |               |                 |                  | HA0 HA1 HA2 X X X X X X X X X X                          | VA0 VA1 VA2 VA3 X X X X X X X X X X          | DA0 DA1 DA2 DA3 DA4 DA5 X X X X X X X X X X | X X X 0 0 1 0 0      |                     | 27 μs               |
| DCRAM data write (*7)   |               |                 |                  |  | AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7              | DA0 DA1 DA2 DA3 DA4 DA5 X X X X X X X X X X | IM1 IM2 X 0 0 1 0 1  |                     | 27 μs/ti μs (*8)    |
| ALATCH data write       |               |                 |                  |  | AD1 AD2 ... AD24 AD25 AD26 ... AD56          | AD57 AD58 AD59 AD60 AD61 AD62 AD63 AD64     | X X X 0 0 1 1 0      |                     | 0 μs                |
| CGRAM data write (*9)   |               |                 |                  | CD1 CD2 ... CD32 CD33 CD34 CD35 CD36 CD37 CD38 CD39 CD40 | CD41 CD42 CD43 CD44 CD45 X X X X X X X X X X | CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7             | WM X X 0 0 1 1 1     |                     | 27 μs/40.5 μs (*10) |
| Set display contrast    |               |                 |                  |  |  | CT0 CT1 CT2 CT3 X X X X X X X X X X         | CTC X X 0 1 0 0 0    |                     | 0 μs                |

X: don't care

Notes \*4: The execution times listed here apply when fosc = 300 kHz. The execution times differ when the oscillator frequency fosc differs.

Example: When fosc = 210 kHz

$$27 \mu s \times \frac{300}{210} = 39 \mu s \quad 162 \mu s \times \frac{300}{210} = 232 \mu s \quad t_i \mu s \times \frac{300}{210} = t_i \times 1.43 \mu s \quad 40.5 \mu s \times \frac{300}{210} = 58 \mu s$$

- \*5: Note that when the power saving mode (BU = 1) is set, the execution time is 27 μs (when fosc = 300 kHz).
- \*6: The execution time must be seen as being 162 μs (when fosc = 300 kHz) if another "display scroll" instruction is executed immediately after a preceding "display scroll" instruction.
- \*7, \*8: Note that the data format differs when a "DCRAM data write" instruction is executed in normal increment mode (IM1 = 1, IM2 = 0) or super-increment mode (IM1 = 0, IM2 = 1). Also note that the execution time is ti μs (when fosc = 300 kHz) if a "DCRAM data write" instruction is executed in super-increment mode. (See detailed instruction descriptions.)
- \*9, \*10: Note that the data format differs when a "CGRAM data write" instruction is executed in double write mode (WM = 1). Also note that the execution time is 40.5 μs (when fosc = 300 kHz) if a "CGRAM data write" instruction is executed in double write mode. (See detailed instruction descriptions.)

**Detailed Instruction Descriptions**

• Set display technique ... <Sets the display technique.>

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| OZ1  | OZ2  | DW   | X    | X    | X    | X    | X    | DT1  | DT2  | FC   | 0    | 0    | 0    | 0    | 1    |

X:don't care

DT1, DT2: Set the display technique

| DT1 | DT2 | Display technique         | Output pins |           |
|-----|-----|---------------------------|-------------|-----------|
|     |     |                           | S80/COM9    | S79/COM10 |
| 0   | 0   | 1/8 duty, 1/4 bias drive  | S80         | S79       |
| 1   | 0   | 1/9 duty, 1/4 bias drive  | COM9        | S79       |
| 0   | 1   | 1/10 duty, 1/4 bias drive | COM9        | COM10     |

\*11: Sn (n = 79, 80): Segment output  
COMn (n = 9, 10): Common output

FC: Set the frame frequency of the common and segment output waveforms

| FC | Frame frequency                 |                                 |                                   |
|----|---------------------------------|---------------------------------|-----------------------------------|
|    | 1/8 duty, 1/4 bias drive f8[Hz] | 1/9 duty, 1/4 bias drive f9[Hz] | 1/10 duty, 1/4 bias drive f10[Hz] |
| 0  | $\frac{f_{osc}}{3072}$          | $\frac{f_{osc}}{3456}$          | $\frac{f_{osc}}{3840}$            |
| 1  | $\frac{f_{osc}}{1536}$          | $\frac{f_{osc}}{1728}$          | $\frac{f_{osc}}{1920}$            |

OZ1, OZ2: Set the display structure

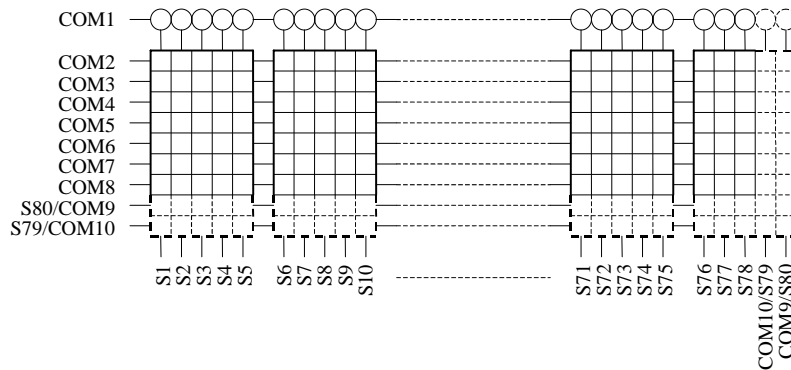
| OZ1 | OZ2 | Display structure                     |
|-----|-----|---------------------------------------|
| 0   | 0   | 64 digits × 1 line display structure  |
| 1   | 0   | 32 digits × 2 lines display structure |
| 0   | 1   | 16 digits × 4 lines display structure |

\*12: See block functions (DCRAM)

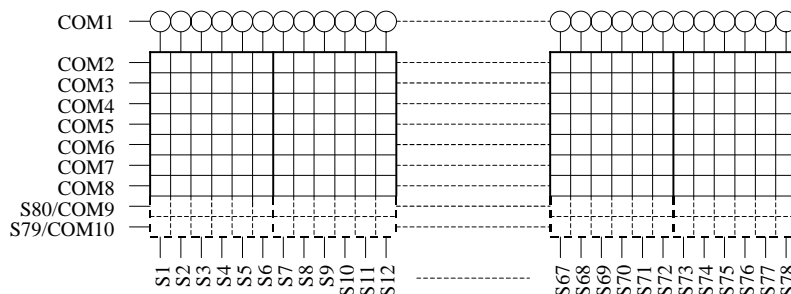
DW: Set the dot font width

| DW | Dot font width   | Number of display digits  |
|----|------------------|---|
| 0  | 5-dot font width | 16 digits × 1 line (5 × 7 dots), 15 digits × 1 line (5 × 8 or 5 × 9 dots) |
| 1  | 6-dot font width | 13 digits × 1 line (6 × 7, 6 × 8, or 6 × 9 dots)                          |

\*13: • 5-dot font width (5 × 7, 5 × 8, or 5 × 9 dots)



• 6-dot font width (6 × 7, 6 × 8, or 6 × 9 dots)



## LC75810E/T

• Display on/off control ... <Turns the display on or off.>

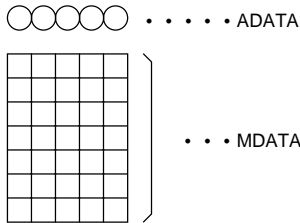
| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D120 | D121 | D122 | D123 | D124 | D125 | D126 | D127 | D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| DG1  | DG2  | DG3  | DG4  | DG5  | DG6  | DG7  | DG8  | DG9  | DG10 | DG11 | DG12 | DG13 | DG14 | DG15 | DG16 | M    | A    | SC   | BU   | 0    | 0    | 1    | 0    |

M, A: Specifies the data to be turned on or off.

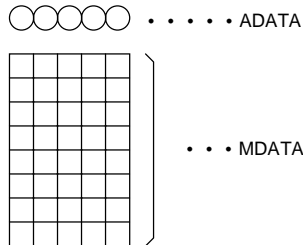
| M | A | Display operating state  |
|---|---|--|
| 0 | 0 | Both MDATA and ADATA are turned off. (The display is forcibly turned off, regardless of the DG1 to DG16 data.)               |
| 0 | 1 | Only ADATA is turned on. (The ADATA of display digits specified by the DG1 to DG16 data are turned on.)                      |
| 1 | 0 | Only MDATA is turned on. (The MDATA of display digits specified by the DG1 to DG16 data are turned on.)                      |
| 1 | 1 | Both MDATA and ADATA are turned on. (The MDATA and ADATA of display digits specified by the DG1 to DG16 data are turned on.) |

\*14: MDATA, ADATA

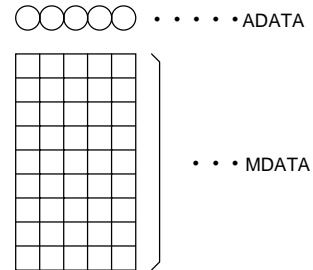
5 × 7 dot matrix



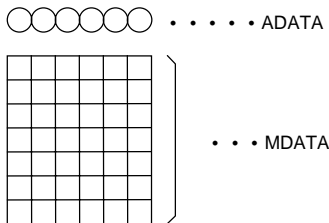
5 × 8 dot matrix



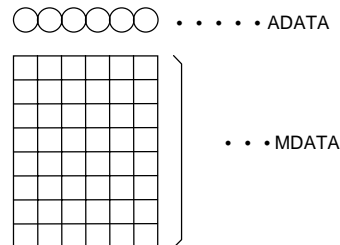
5 × 9 dot matrix



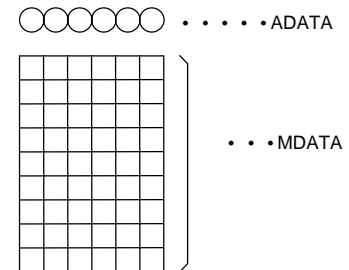
6 × 7 dot matrix



6 × 8 dot matrix



6 × 9 dot matrix



DG1 to DG16: Specifies the display digit.

| Display digit      | 1   | 2   | 3   | 4   | 5   | 6   | 7   | 8   | 9   | 10   | 11   | 12   | 13   | 14   | 15   | 16   |
|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|
| Display digit data | DG1 | DG2 | DG3 | DG4 | DG5 | DG6 | DG7 | DG8 | DG9 | DG10 | DG11 | DG12 | DG13 | DG14 | DG15 | DG16 |

For example, if DG1 to DG8 are 1, and DG9 to DG16 are 0, then display digits 1 to 8 will be turned on, and display digits 9 to 16 will be turned off (blanked).

SC: Controls the common and segment output pins.

| SC | Common and segment output pin states           |
|----|--|
| 0  | Output of LCD drive waveforms                  |
| 1  | Fixed at the $V_{SS}$ level (all segments off) |

Note \*15: When SC is 1, the S1 to S8 and COM1 to COM10 output pins are set to the  $V_{SS}$  level, regardless of the M, A, and DG1 to DG16 data.

BU: Controls the normal mode and power saving mode.

| BU | Mode   |
|----|--|
| 0  | Normal mode  |
| 1  | Power saving mode<br>(In this mode, the OSC pin oscillator is stopped, and the common and segment pins are set to the $V_{SS}$ level. In this mode, instructions other than the "display on/off control" and "set display contrast" instructions cannot be executed. Thus applications must set the IC to normal mode before executing any of the other instructions.) |

## LC75810E/T

- Display scroll ... <Scrolls the display smoothly.>

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D120 | D121 | D122 | D123 | D124 | D125 | D126 | D127 | D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| HS0  | HS1  | HS2  | X    | X    | X    | X    | X    | VS0  | VS1  | VS2  | VS3  | X    | X    | X    | X    | R/L  | D/U  | X    | 0    | 0    | 0    | 1    | 1    |

X: don't care

HS0 to HS2: Set the amount of smooth scrolling to be applied to MDATA in the left/right direction.

| HS0 | HS1 | HS2 | Amount of smooth scrolling to be applied to MDATA in the left/right direction                            |
|-----|-----|-----|--|
| 0   | 0   | 0   | No shift in either the left or right direction   |
| 1   | 0   | 0   | Shift 1 dot to the left or right. (The shift direction (left or right) is specified with the R/L data.)  |
| 0   | 1   | 0   | Shift 2 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.) |
| 1   | 1   | 0   | Shift 3 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.) |
| 0   | 0   | 1   | Shift 4 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.) |
| 1   | 0   | 1   | Shift 5 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.) |
| 0   | 1   | 1   | Shift 6 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.) |

VS0 to VS3: Set the amount of smooth scrolling to be applied to MDATA in the up/down direction.

| VS0 | VS1 | VS2 | VS3 | Amount of smooth scrolling to be applied to MDATA in the up/down direction                                |
|-----|-----|-----|-----|---|
| 0   | 0   | 0   | 0   | No shift in either the up or down direction   |
| 1   | 0   | 0   | 0   | Shift 1 dot to the up or down. (The shift direction (up or down) is specified with the D/U data.)         |
| 0   | 1   | 0   | 0   | Shift 2 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)        |
| 1   | 1   | 0   | 0   | Shift 3 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)        |
| 0   | 0   | 1   | 0   | Shift 4 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)        |
| 1   | 0   | 1   | 0   | Shift 5 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)        |
| 0   | 1   | 1   | 0   | Shift 6 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)        |
| 1   | 1   | 1   | 0   | Shift 7 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)        |
| 0   | 0   | 0   | 1   | Shift 8 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)        |
| 1   | 0   | 0   | 1   | Shift 9 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.) (*16)  |
| 0   | 1   | 0   | 1   | Shift 10 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.) (*17) |

Notes: \*16: This shift cannot be used when MDATA is 5 × 7 or 6 × 7 dots.

\*17: This shift cannot be used when MDATA is 5 × 7, 5 × 8, 6 × 7 or 6 × 8 dots.

R/L: Specifies the MDATA shift direction (left or right).

| R/L | MDATA shift direction (left or right) |
|-----|---------------------------------------|
| 0   | Shift left                            |
| 1   | Shift right                           |

D/U: Specifies the MDATA shift direction (up or down).

| D/U | MDATA shift direction (up or down) |
|-----|------------------------------------|
| 0   | Shift up                           |
| 1   | Shift down                         |

\*18 Example of the “display scroll” instruction execution

Assume that a 32 digits × 2 lines display structure (OZ1 = 1, OZ2 = 0) has been set up with the “set display technique” instruction, and that the following data has been written to DCRAM with the “DCRAM data write” instruction.

| Display digit | 1           | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |   |
|---------------|-------------|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|
| DCRAM data    | First line  | A | B | C | D | E | F | G | H | I  | J  | K  | L  | M  | N  | O  | P  | Q  | R  | S  | T  | U  | V  | W  | X  | Y  | Z  | <  | >  | z  | y  | x  | w |
|               | Second line | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8  | 9  | a  | b  | c  | d  | e  | f  | g  | h  | i  | j  | k  | l  | m  | n  | o  | p  | q  | r  | s  | t  | u  | v |

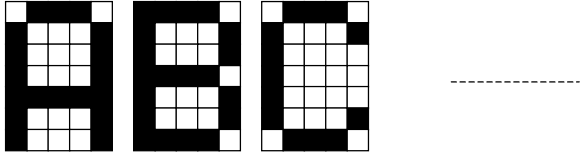
• Display state (1)

With no shifting in any direction, left, right, up, or down.

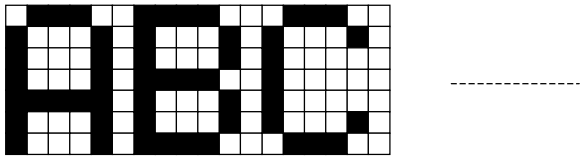
| HS0 | HS1 | HS2 | VS0 | VS1 | VS2 | VS3 | R/L | D/U |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | X   | X   |

X: don't care

(5 × 7 dot matrix)



(6 × 7 dot matrix)

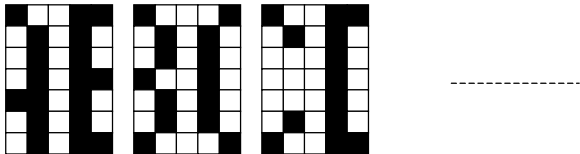


• Display state (2)

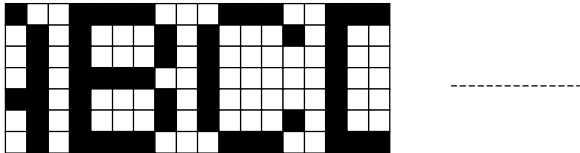
Shifted 3 dots to the left relative to display state (1)

| HS0 | HS1 | HS2 | VS0 | VS1 | VS2 | VS3 | R/L | D/U |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1   | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

(5 × 7 dot matrix)



(6 × 7 dot matrix)

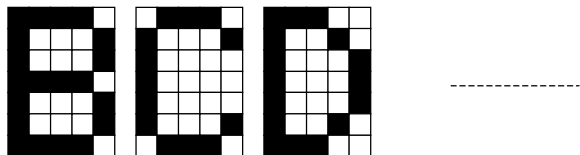


• Display state (3)

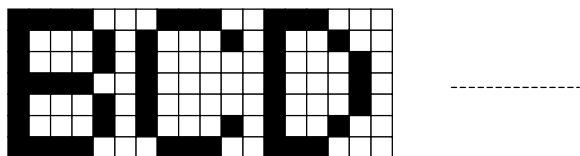
Shifted 6 dots to the left relative to display state (1)

| HS0 | HS1 | HS2 | VS0 | VS1 | VS2 | VS3 | R/L | D/U |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 1   | 1   | 0   | 0   | 0   | 0   | 0   | 0   |

(5 × 7 dot matrix)



(6 × 7 dot matrix)



Shifted 3 dots to the left relative to display state (2)

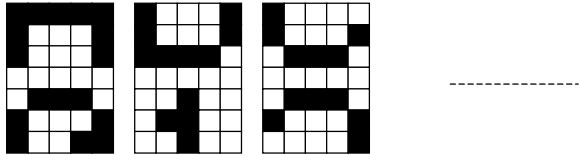
| HS0 | HS1 | HS2 | VS0 | VS1 | VS2 | VS3 | R/L | D/U |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1   | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

• Display state (4)

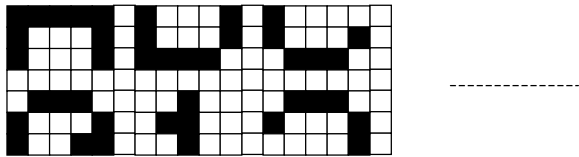
Shifted 4 dots to the up relative to display state (1)

| HS0 | HS1 | HS2 | VS0 | VS1 | VS2 | VS3 | R/L | D/U |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   | 1   | 0   | 0   | 0   |

(5 × 7 dot matrix)



(6 × 7 dot matrix)

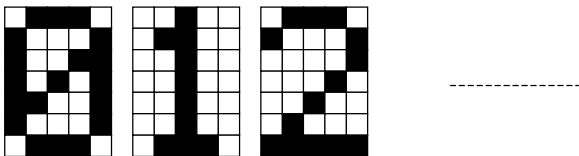


• Display state (5)

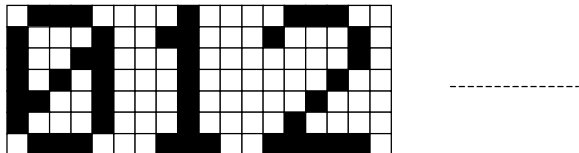
Shifted 8 dots to the up relative to display state (1)

| HS0 | HS1 | HS2 | VS0 | VS1 | VS2 | VS3 | R/L | D/U |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   | 0   | 1   | 0   | 0   |

(5 × 7 dot matrix)



(6 × 7 dot matrix)



Shifted 4 dots to the up relative to display state (4)

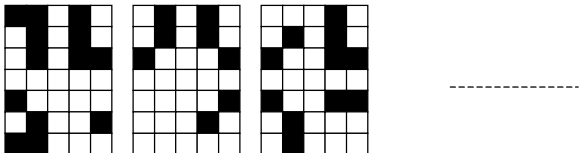
| HS0 | HS1 | HS2 | VS0 | VS1 | VS2 | VS3 | R/L | D/U |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   | 1   | 0   | 0   | 0   |

• Display state (6)

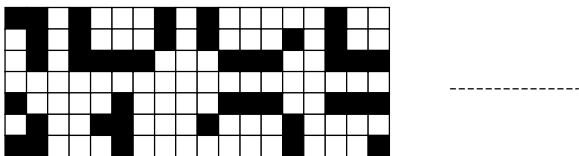
Shifted 3 dots to the left and 4 dots to the up relative to display state (1)

| HS0 | HS1 | HS2 | VS0 | VS1 | VS2 | VS3 | R/L | D/U |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1   | 1   | 0   | 0   | 0   | 1   | 0   | 0   | 0   |

(5 × 7 dot matrix)



(6 × 7 dot matrix)

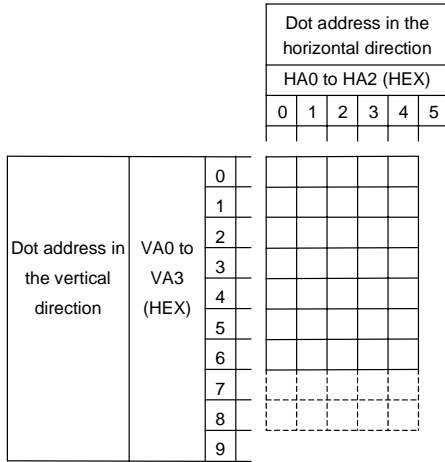






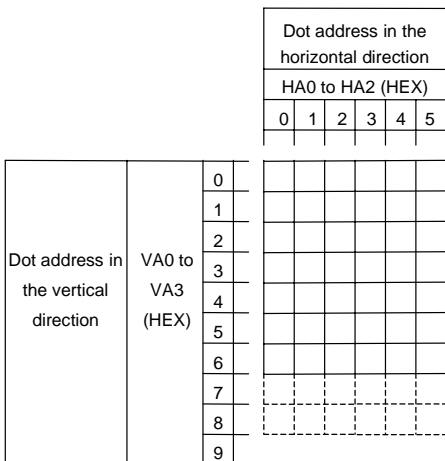
\*19 The figure below lists the correspondence between the data HA0 to HA2 which is dot address in the horizontal direction and the dot matrix character pattern, and the correspondence between the data VA0 to VA3 which is dot address in the vertical direction and the dot matrix character pattern.

• 5-dot font width: 5 × 7, 5 × 8, or 5 × 9 dots



- The area at HA0 to 2 = 5H is allocated to the space at the right of the dot matrix character pattern.
- The area at VA0 to 3 = 7H, for 5 × 7 dot characters, is allocated to the space at the bottom of the dot matrix character pattern.
- The area at VA0 to 3 = 8H is illegal for 5 × 7 dot characters. For 5 × 8 dot characters, it is allocated to the space at the bottom of the dot matrix character pattern.
- The area at VA0 to 3 = 9H is illegal for 5 × 7 or 5 × 8 dot characters. For 5 × 9 dot characters, it is allocated to the space at the bottom of the dot matrix character pattern.

• 6-dot font width: 6 × 7, 6 × 8, or 6 × 9 dots



- The area at HA0 to 2 = 5H is allocated to the space at the right of the dot matrix character pattern.
- The area at VA0 to 3 = 7H, for 6 × 7 dot characters, is allocated to the space at the bottom of the dot matrix character pattern.
- The area at VA0 to 3 = 8H is illegal for 6 × 7 dot characters. For 6 × 8 dot characters, it is allocated to the space at the bottom of the dot matrix character pattern.
- The area at VA0 to 3 = 9H is illegal for 6 × 7 or 6 × 8 dot characters. For 6 × 9 dot characters, it is allocated to the space at the bottom of the dot matrix character pattern.

\*20: Example of the “set AC and SC addresses” instruction execution

Assume that a 32 digits × 2 lines display structure (OZ1 = 1, OZ2 = 0) has been set up with the “set display technique” instruction, and that the following data has been written to DCRAM with the “DCRAM data write” instruction.

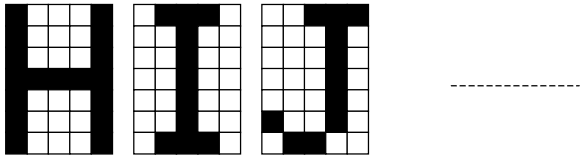
|               |   |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|---------------|---|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| Display digit |   | 1      | 2      | 3      | 4      | 5      | 6      | 7      | 8      | 9      | 10     | 11     | 12     | 13     | 14     | 15     | 16     |
| DCRAM data    | First line (DCRAM address (hexadecimal))  | A (00) | B (01) | C (02) | D (03) | E (04) | F (05) | G (06) | H (07) | I (08) | J (09) | K (0A) | L (0B) | M (0C) | N (0D) | O (0E) | P (0F) |
|               | Second line (DCRAM address (hexadecimal)) | 0 (20) | 1 (21) | 2 (22) | 3 (23) | 4 (24) | 5 (25) | 6 (26) | 7 (27) | 8 (28) | 9 (29) | a (2A) | b (2B) | c (2C) | d (2D) | e (2E) | f (2F) |

|               |   |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|---------------|---|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| Display digit |   | 17     | 18     | 19     | 20     | 21     | 22     | 23     | 24     | 25     | 26     | 27     | 28     | 29     | 30     | 31     | 32     |
| DCRAM data    | First line (DCRAM address (hexadecimal))  | Q (10) | R (11) | S (12) | T (13) | U (14) | V (15) | W (16) | X (17) | Y (18) | Z (19) | < (1A) | > (1B) | z (1C) | y (1D) | x (1E) | w (1F) |
|               | Second line (DCRAM address (hexadecimal)) | g (30) | h (31) | i (32) | j (33) | k (34) | l (35) | m (36) | n (37) | o (38) | p (39) | q (3A) | r (3B) | s (3C) | t (3D) | u (3E) | v (3F) |

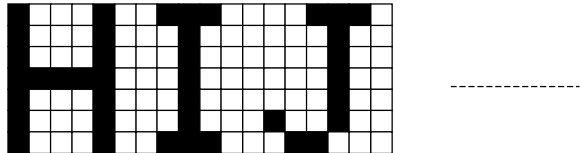
- When DA0 to 5 is set to 07H, HA0 to 2 is set to 0H, and VA0 to 3 is set to 0H.

| HA0 | HA1 | HA2 | VA0 | VA1 | VA2 | VA3 | DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 1   | 0   | 0   | 0   |

(5 × 7 dot matrix)



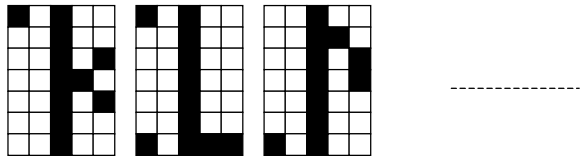
(6 × 7 dot matrix)



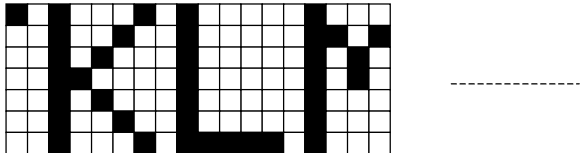
- When DA0 to 5 is set to 09H, HA0 to 2 is set to 4H, and VA0 to 3 is set to 0H.

| HA0 | HA1 | HA2 | VA0 | VA1 | VA2 | VA3 | DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 0   | 1   | 0   | 0   | 0   | 0   | 1   | 0   | 0   | 1   | 0   | 0   |

(5 × 7 dot matrix)



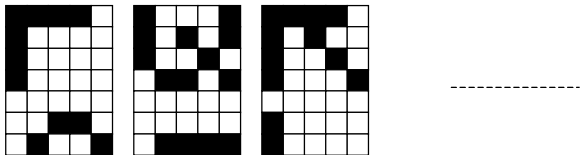
(6 × 7 dot matrix)



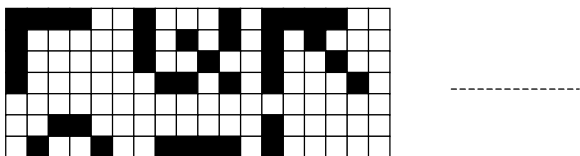
- When DA0 to 5 is set to 0FH, HA0 to 2 is set to 0H, and VA0 to 3 is set to 3H.

| HA0 | HA1 | HA2 | VA0 | VA1 | VA2 | VA3 | DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 1   | 1   | 0   | 0   | 1   | 1   | 1   | 1   | 0   | 0   |

(5 × 7 dot matrix)



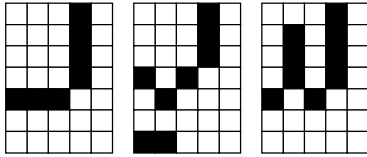
(6 × 7 dot matrix)



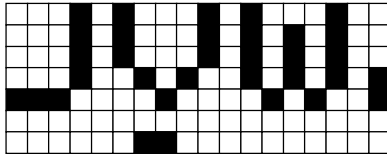
- When DA0 to 5 is set to 14H, HA0 to 2 is set to 1H, and VA0 to 3 is set to 2H.

| HA0 | HA1 | HA2 | VA0 | VA1 | VA2 | VA3 | DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1   | 0   | 0   | 0   | 1   | 0   | 0   | 0   | 0   | 1   | 0   | 1   | 0   |

(5 × 7 dot matrix)



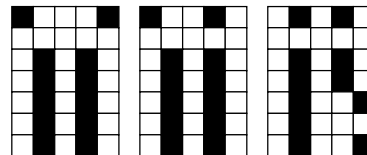
(6 × 7 dot matrix)



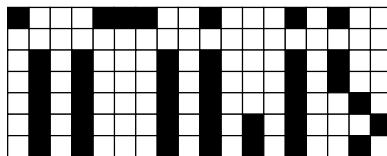
- When DA0 to 5 is set to 34H, HA0 to 2 is set to 3H, and VA0 to 3 is set to 6H.

| HA0 | HA1 | HA2 | VA0 | VA1 | VA2 | VA3 | DA0 | DA1 | DA2 | DA3 | DA4 | DA5 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1   | 1   | 0   | 0   | 1   | 1   | 0   | 0   | 0   | 1   | 0   | 1   | 1   |

(5 × 7 dot matrix)



(6 × 7 dot matrix)



- DCRAM data write ... <Specifies the DCRAM address and stores data at that address.>

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D120 | D121 | D122 | D123 | D124 | D125 | D126 | D127 | D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| AC0  | AC1  | AC2  | AC3  | AC4  | AC5  | AC6  | AC7  | DA0  | DA1  | DA2  | DA3  | DA4  | DA5  | X    | X    | IM1  | IM2  | X    | 0    | 0    | 1    | 0    | 1    |

X: don't care

DA0 to DA5: DCRAM address

| DA0                   | DA1 | DA2 | DA3                  | DA4 | DA5 |
|-----------------------|-----|-----|----------------------|-----|-----|
| LSB                   |     |     | MSB                  |     |     |
| ↑                     |     |     | ↑                    |     |     |
| Least significant bit |     |     | Most significant bit |     |     |

AC0 to AC7: DCRAM data (character code)

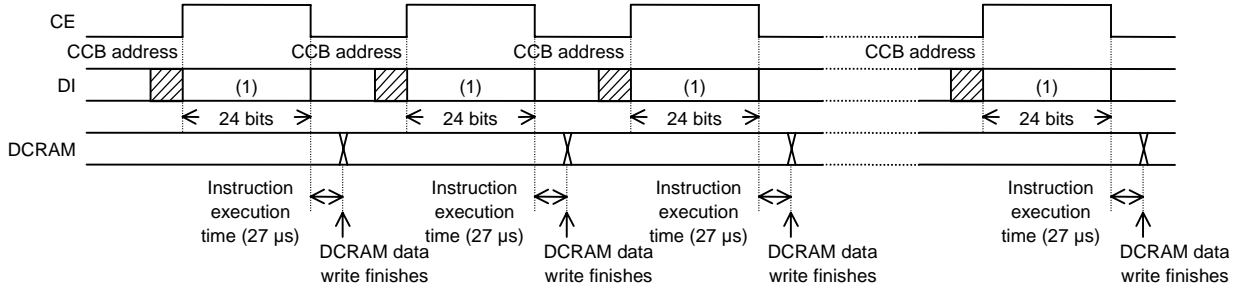
| AC0                   | AC1 | AC2 | AC3 | AC4                  | AC5 | AC6 | AC7 |
|-----------------------|-----|-----|-----|----------------------|-----|-----|-----|
| LSB                   |     |     |     | MSB                  |     |     |     |
| ↑                     |     |     |     | ↑                    |     |     |     |
| Least significant bit |     |     |     | Most significant bit |     |     |     |

This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code, and is converted to a 5 × 7, 5 × 8, or 5 × 9 dot matrix display data using CGROM or CGRAM.

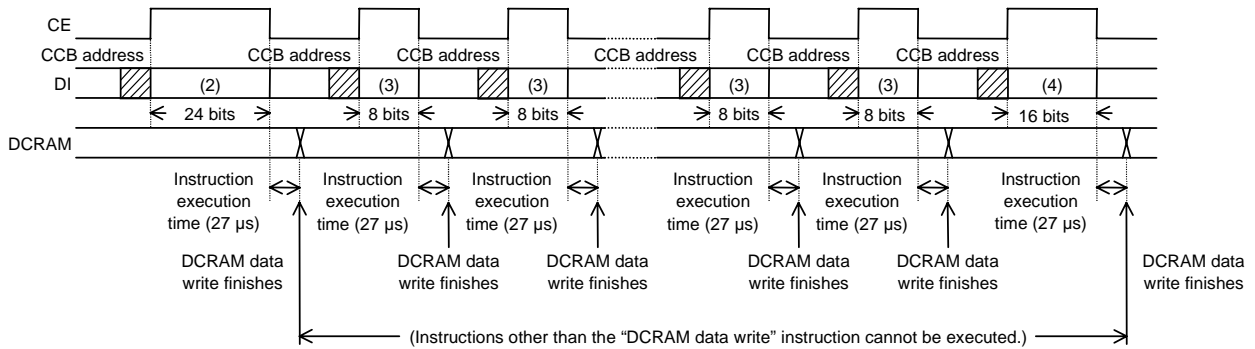
IM1 and IM2: Sets the method of writing data to DCRAM

| IM1 | IM2 | DCRAM data write method   |
|-----|-----|---|
| 0   | 0   | Normal DCRAM data write (Specifies the DCRAM address and writes the DCRAM data.)                                |
| 1   | 0   | Normal increment mode DCRAM data write (Increments the DCRAM address by +1 each time data is written to DCRAM.) |
| 0   | 1   | Super-increment mode DCRAM data write (Writes 2 to 16 characters of DCRAM data in a single operation.)          |

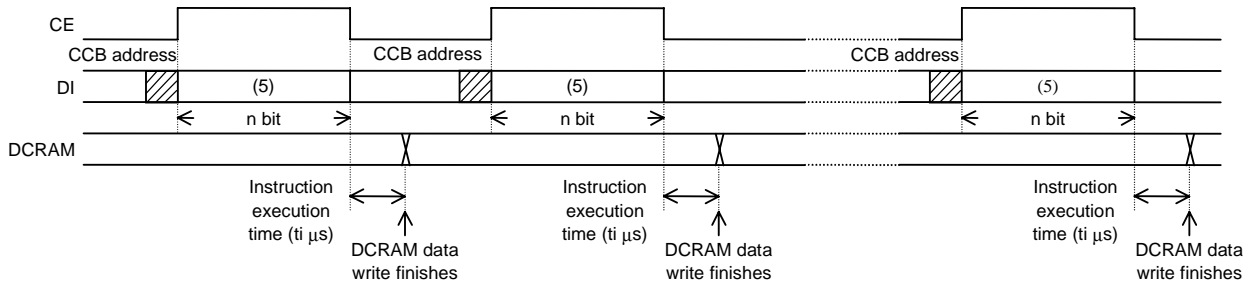
\*21 • DCRAM data write method when IM1 is 0 and IM2 is 0.



• DCRAM data write method when IM1 is 1 and IM2 is 0.  
(Instructions other than the “DCRAM data write” instruction cannot be executed.)



• DCRAM data write method when IM1 is 0 and IM2 is 1.



$t_i = 13.5\mu s \times (\frac{n}{8} - 1)$  ( $n = 8m + 16$ ,  $m$  is an integer between 2 and 16 that is the number of characters written as DCRAM data.)

- For example When  $n = 32$  bits ( $m = 2$ ):  $t_i = 40.5 \mu s$  (when  $f_{osc} = 300$  kHz)
- When  $n = 80$  bits ( $m = 8$ ):  $t_i = 121.5 \mu s$  (when  $f_{osc} = 300$  kHz)
- When  $n = 144$  bits ( $m = 16$ ):  $t_i = 229.5 \mu s$  (when  $f_{osc} = 300$  kHz)

Note that the instruction execution time of 27 μs and  $t_i$  values in μs apply when  $f_{osc} = 300$  kHz, and that these times will differ when the oscillator frequency  $f_{osc}$  differs.

**LC75810E/T**

Data format (1) (24 bits)

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D120 | D121 | D122 | D123 | D124 | D125 | D126 | D127 | D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| AC0  | AC1  | AC2  | AC3  | AC4  | AC5  | AC6  | AC7  | DA0  | DA1  | DA2  | DA3  | DA4  | DA5  | X    | X    | 0    | 0    | X    | 0    | 0    | 1    | 0    | 1    |

X: don't care

Data format (2) (24 bits)

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D120 | D121 | D122 | D123 | D124 | D125 | D126 | D127 | D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| AC0  | AC1  | AC2  | AC3  | AC4  | AC5  | AC6  | AC7  | DA0  | DA1  | DA2  | DA3  | DA4  | DA5  | X    | X    | 1    | 0    | X    | 0    | 0    | 1    | 0    | 1    |

X: don't care

Data format (3) (8 bits)

| Code |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| AC0  | AC1  | AC2  | AC3  | AC4  | AC5  | AC6  | AC7  |

Data format (4) (16 bits)

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| AC0  | AC1  | AC2  | AC3  | AC4  | AC5  | AC6  | AC7  | 0    | 0    | X    | 0    | 0    | 1    | 0    | 1    |

X: don't care

Data format (5) (n bits)

| Code             |                  |                  |                  |                  |                  |                  |                  |       |       |       |       |       |       |       |       |                    |                    |                    |                    |                    |                    |                    |                    |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------|-------|-------|-------|-------|-------|-------|-------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Dz               | Dz+1             | Dz+2             | Dz+3             | Dz+4             | Dz+5             | Dz+6             | Dz+7             | ..... | ..... | ..... | ..... | ..... | ..... | ..... | ..... | D112               | D113               | D114               | D115               | D116               | D117               | D118               | D119               |
| AC0 <sub>m</sub> | AC1 <sub>m</sub> | AC2 <sub>m</sub> | AC3 <sub>m</sub> | AC4 <sub>m</sub> | AC5 <sub>m</sub> | AC6 <sub>m</sub> | AC7 <sub>m</sub> | ..... | ..... | ..... | ..... | ..... | ..... | ..... | ..... | AC0 <sub>m-1</sub> | AC1 <sub>m-1</sub> | AC2 <sub>m-1</sub> | AC3 <sub>m-1</sub> | AC4 <sub>m-1</sub> | AC5 <sub>m-1</sub> | AC6 <sub>m-1</sub> | AC7 <sub>m-1</sub> |

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |      |      |      |      |      |      |      |      |      |      |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------|------|------|------|------|------|------|------|------|------|
| D120             | D121             | D122             | D123             | D124             | D125             | D126             | D127             | D128             | D129             | D130             | D131             | D132             | D133             | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| AC0 <sub>m</sub> | AC1 <sub>m</sub> | AC2 <sub>m</sub> | AC3 <sub>m</sub> | AC4 <sub>m</sub> | AC5 <sub>m</sub> | AC6 <sub>m</sub> | AC7 <sub>m</sub> | DA0 <sub>i</sub> | DA1 <sub>i</sub> | DA2 <sub>i</sub> | DA3 <sub>i</sub> | DA4 <sub>i</sub> | DA5 <sub>i</sub> | X    | X    | 0    | 1    | X    | 0    | 0    | 1    | 0    | 1    |

X: don't care

Here,  $n = 8m + 16$ ,  $z = 128 - 8m$  ( $m$  is an integer between 2 and 16 that is the number of characters written as DCRAM data.)

Correspondence between the DCRAM address and the DCRAM data

| DCRAM address                                     | DCRAM data                               |
|---|--|
| DA0 <sub>i</sub> to DA5 <sub>i</sub>              | AC0 <sub>i</sub> to AC7 <sub>i</sub>     |
| (DA0 <sub>i</sub> to DA5 <sub>i</sub> ) + 1       | AC0 <sub>2</sub> to AC7 <sub>2</sub>     |
| (DA0 <sub>i</sub> to DA5 <sub>i</sub> ) + 2       | AC0 <sub>3</sub> to AC7 <sub>3</sub>     |
| ⋮   | ⋮  |
| (DA0 <sub>i</sub> to DA5 <sub>i</sub> ) + (m - 3) | AC0 <sub>m-2</sub> to AC7 <sub>m-2</sub> |
| (DA0 <sub>i</sub> to DA5 <sub>i</sub> ) + (m - 2) | AC0 <sub>m-1</sub> to AC7 <sub>m-1</sub> |
| (DA0 <sub>i</sub> to DA5 <sub>i</sub> ) + (m - 1) | AC0 <sub>m</sub> to AC7 <sub>m</sub>     |

## LC75810E/T

Example 1: When n = 32 bits (m = 2: 2 characters DCRAM data write operation)

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D112             | D113             | D114             | D115             | D116             | D117             | D118             | D119             | D120             | D121             | D122             | D123             | D124             | D125             | D126             | D127             |
| AC0 <sub>1</sub> | AC1 <sub>1</sub> | AC2 <sub>1</sub> | AC3 <sub>1</sub> | AC4 <sub>1</sub> | AC5 <sub>1</sub> | AC6 <sub>1</sub> | AC7 <sub>1</sub> | AC0 <sub>2</sub> | AC1 <sub>2</sub> | AC2 <sub>2</sub> | AC3 <sub>2</sub> | AC4 <sub>2</sub> | AC5 <sub>2</sub> | AC6 <sub>2</sub> | AC7 <sub>2</sub> |

| Code             |                  |                  |                  |                  |                  |      |      |      |      |      |      |      |      |      |      |
|------------------|------------------|------------------|------------------|------------------|------------------|------|------|------|------|------|------|------|------|------|------|
| D128             | D129             | D130             | D131             | D132             | D133             | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| DA0 <sub>1</sub> | DA1 <sub>1</sub> | DA2 <sub>1</sub> | DA3 <sub>1</sub> | DA4 <sub>1</sub> | DA5 <sub>1</sub> | X    | X    | 0    | 1    | X    | 0    | 0    | 1    | 0    | 1    |

X: don't care

Correspondence between the DCRAM address and the DCRAM data

| DCRAM address                               | DCRAM data                           |
|---|--------------------------------------|
| DA0 <sub>1</sub> to DA5 <sub>1</sub>        | AC0 <sub>1</sub> to AC7 <sub>1</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 1 | AC0 <sub>2</sub> to AC7 <sub>2</sub> |

Example 2: When n = 80 bits (m = 8: 8 characters DCRAM data write operation)

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D64              | D65              | D66              | D67              | D68              | D69              | D70              | D71              | D72              | D73              | D74              | D75              | D76              | D77              | D78              | D79              |
| AC0 <sub>1</sub> | AC1 <sub>1</sub> | AC2 <sub>1</sub> | AC3 <sub>1</sub> | AC4 <sub>1</sub> | AC5 <sub>1</sub> | AC6 <sub>1</sub> | AC7 <sub>1</sub> | AC0 <sub>2</sub> | AC1 <sub>2</sub> | AC2 <sub>2</sub> | AC3 <sub>2</sub> | AC4 <sub>2</sub> | AC5 <sub>2</sub> | AC6 <sub>2</sub> | AC7 <sub>2</sub> |

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D80              | D81              | D82              | D83              | D84              | D85              | D86              | D87              | D88              | D89              | D90              | D91              | D92              | D93              | D94              | D95              |
| AC0 <sub>3</sub> | AC1 <sub>3</sub> | AC2 <sub>3</sub> | AC3 <sub>3</sub> | AC4 <sub>3</sub> | AC5 <sub>3</sub> | AC6 <sub>3</sub> | AC7 <sub>3</sub> | AC0 <sub>4</sub> | AC1 <sub>4</sub> | AC2 <sub>4</sub> | AC3 <sub>4</sub> | AC4 <sub>4</sub> | AC5 <sub>4</sub> | AC6 <sub>4</sub> | AC7 <sub>4</sub> |

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D96              | D97              | D98              | D99              | D100             | D101             | D102             | D103             | D104             | D105             | D106             | D107             | D108             | D109             | D110             | D111             |
| AC0 <sub>5</sub> | AC1 <sub>5</sub> | AC2 <sub>5</sub> | AC3 <sub>5</sub> | AC4 <sub>5</sub> | AC5 <sub>5</sub> | AC6 <sub>5</sub> | AC7 <sub>5</sub> | AC0 <sub>6</sub> | AC1 <sub>6</sub> | AC2 <sub>6</sub> | AC3 <sub>6</sub> | AC4 <sub>6</sub> | AC5 <sub>6</sub> | AC6 <sub>6</sub> | AC7 <sub>6</sub> |

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D112             | D113             | D114             | D115             | D116             | D117             | D118             | D119             | D120             | D121             | D122             | D123             | D124             | D125             | D126             | D127             |
| AC0 <sub>7</sub> | AC1 <sub>7</sub> | AC2 <sub>7</sub> | AC3 <sub>7</sub> | AC4 <sub>7</sub> | AC5 <sub>7</sub> | AC6 <sub>7</sub> | AC7 <sub>7</sub> | AC0 <sub>8</sub> | AC1 <sub>8</sub> | AC2 <sub>8</sub> | AC3 <sub>8</sub> | AC4 <sub>8</sub> | AC5 <sub>8</sub> | AC6 <sub>8</sub> | AC7 <sub>8</sub> |

| Code             |                  |                  |                  |                  |                  |      |      |      |      |      |      |      |      |      |      |
|------------------|------------------|------------------|------------------|------------------|------------------|------|------|------|------|------|------|------|------|------|------|
| D128             | D129             | D130             | D131             | D132             | D133             | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| DA0 <sub>1</sub> | DA1 <sub>1</sub> | DA2 <sub>1</sub> | DA3 <sub>1</sub> | DA4 <sub>1</sub> | DA5 <sub>1</sub> | X    | X    | 0    | 1    | X    | 0    | 0    | 1    | 0    | 1    |

X: don't care

Correspondence between the DCRAM address and the DCRAM data

| DCRAM address                               | DCRAM data                           |
|---|--------------------------------------|
| DA0 <sub>1</sub> to DA5 <sub>1</sub>        | AC0 <sub>1</sub> to AC7 <sub>1</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 1 | AC0 <sub>2</sub> to AC7 <sub>2</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 2 | AC0 <sub>3</sub> to AC7 <sub>3</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 3 | AC0 <sub>4</sub> to AC7 <sub>4</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 4 | AC0 <sub>5</sub> to AC7 <sub>5</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 5 | AC0 <sub>6</sub> to AC7 <sub>6</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 6 | AC0 <sub>7</sub> to AC7 <sub>7</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 7 | AC0 <sub>8</sub> to AC7 <sub>8</sub> |

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Example 3: When n = 144 bits (m = 16: 16 characters DCRAM data write operation)

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D0               | D1               | D2               | D3               | D4               | D5               | D6               | D7               | D8               | D9               | D10              | D11              | D12              | D13              | D14              | D15              |
| AC0 <sub>0</sub> | AC1 <sub>0</sub> | AC2 <sub>0</sub> | AC3 <sub>0</sub> | AC4 <sub>0</sub> | AC5 <sub>0</sub> | AC6 <sub>0</sub> | AC7 <sub>0</sub> | AC0 <sub>1</sub> | AC1 <sub>1</sub> | AC2 <sub>1</sub> | AC3 <sub>1</sub> | AC4 <sub>1</sub> | AC5 <sub>1</sub> | AC6 <sub>1</sub> | AC7 <sub>1</sub> |

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D16              | D17              | D18              | D19              | D20              | D21              | D22              | D23              | D24              | D25              | D26              | D27              | D28              | D29              | D30              | D31              |
| AC0 <sub>3</sub> | AC1 <sub>3</sub> | AC2 <sub>3</sub> | AC3 <sub>3</sub> | AC4 <sub>3</sub> | AC5 <sub>3</sub> | AC6 <sub>3</sub> | AC7 <sub>3</sub> | AC0 <sub>4</sub> | AC1 <sub>4</sub> | AC2 <sub>4</sub> | AC3 <sub>4</sub> | AC4 <sub>4</sub> | AC5 <sub>4</sub> | AC6 <sub>4</sub> | AC7 <sub>4</sub> |

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D32              | D33              | D34              | D35              | D36              | D37              | D38              | D39              | D40              | D41              | D42              | D43              | D44              | D45              | D46              | D47              |
| AC0 <sub>5</sub> | AC1 <sub>5</sub> | AC2 <sub>5</sub> | AC3 <sub>5</sub> | AC4 <sub>5</sub> | AC5 <sub>5</sub> | AC6 <sub>5</sub> | AC7 <sub>5</sub> | AC0 <sub>6</sub> | AC1 <sub>6</sub> | AC2 <sub>6</sub> | AC3 <sub>6</sub> | AC4 <sub>6</sub> | AC5 <sub>6</sub> | AC6 <sub>6</sub> | AC7 <sub>6</sub> |

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D48              | D49              | D50              | D51              | D52              | D53              | D54              | D55              | D56              | D57              | D58              | D59              | D60              | D61              | D62              | D63              |
| AC0 <sub>7</sub> | AC1 <sub>7</sub> | AC2 <sub>7</sub> | AC3 <sub>7</sub> | AC4 <sub>7</sub> | AC5 <sub>7</sub> | AC6 <sub>7</sub> | AC7 <sub>7</sub> | AC0 <sub>8</sub> | AC1 <sub>8</sub> | AC2 <sub>8</sub> | AC3 <sub>8</sub> | AC4 <sub>8</sub> | AC5 <sub>8</sub> | AC6 <sub>8</sub> | AC7 <sub>8</sub> |

| Code             |                  |                  |                  |                  |                  |                  |                  |                   |                   |                   |                   |                   |                   |                   |                   |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D64              | D65              | D66              | D67              | D68              | D69              | D70              | D71              | D72               | D73               | D74               | D75               | D76               | D77               | D78               | D79               |
| AC0 <sub>9</sub> | AC1 <sub>9</sub> | AC2 <sub>9</sub> | AC3 <sub>9</sub> | AC4 <sub>9</sub> | AC5 <sub>9</sub> | AC6 <sub>9</sub> | AC7 <sub>9</sub> | AC0 <sub>10</sub> | AC1 <sub>10</sub> | AC2 <sub>10</sub> | AC3 <sub>10</sub> | AC4 <sub>10</sub> | AC5 <sub>10</sub> | AC6 <sub>10</sub> | AC7 <sub>10</sub> |

| Code              |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D80               | D81               | D82               | D83               | D84               | D85               | D86               | D87               | D88               | D89               | D90               | D91               | D92               | D93               | D94               | D95               |
| AC0 <sub>11</sub> | AC1 <sub>11</sub> | AC2 <sub>11</sub> | AC3 <sub>11</sub> | AC4 <sub>11</sub> | AC5 <sub>11</sub> | AC6 <sub>11</sub> | AC7 <sub>11</sub> | AC0 <sub>12</sub> | AC1 <sub>12</sub> | AC2 <sub>12</sub> | AC3 <sub>12</sub> | AC4 <sub>12</sub> | AC5 <sub>12</sub> | AC6 <sub>12</sub> | AC7 <sub>12</sub> |

| Code              |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D96               | D97               | D98               | D99               | D100              | D101              | D102              | D103              | D104              | D105              | D106              | D107              | D108              | D109              | D110              | D111              |
| AC0 <sub>13</sub> | AC1 <sub>13</sub> | AC2 <sub>13</sub> | AC3 <sub>13</sub> | AC4 <sub>13</sub> | AC5 <sub>13</sub> | AC6 <sub>13</sub> | AC7 <sub>13</sub> | AC0 <sub>14</sub> | AC1 <sub>14</sub> | AC2 <sub>14</sub> | AC3 <sub>14</sub> | AC4 <sub>14</sub> | AC5 <sub>14</sub> | AC6 <sub>14</sub> | AC7 <sub>14</sub> |

| Code              |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D112              | D113              | D114              | D115              | D116              | D117              | D118              | D119              | D120              | D121              | D122              | D123              | D124              | D125              | D126              | D127              |
| AC0 <sub>15</sub> | AC1 <sub>15</sub> | AC2 <sub>15</sub> | AC3 <sub>15</sub> | AC4 <sub>15</sub> | AC5 <sub>15</sub> | AC6 <sub>15</sub> | AC7 <sub>15</sub> | AC0 <sub>16</sub> | AC1 <sub>16</sub> | AC2 <sub>16</sub> | AC3 <sub>16</sub> | AC4 <sub>16</sub> | AC5 <sub>16</sub> | AC6 <sub>16</sub> | AC7 <sub>16</sub> |

| Code             |                  |                  |                  |                  |                  |      |      |      |      |      |      |      |      |      |      |
|------------------|------------------|------------------|------------------|------------------|------------------|------|------|------|------|------|------|------|------|------|------|
| D128             | D129             | D130             | D131             | D132             | D133             | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| DA0 <sub>1</sub> | DA1 <sub>1</sub> | DA2 <sub>1</sub> | DA3 <sub>1</sub> | DA4 <sub>1</sub> | DA5 <sub>1</sub> | X    | X    | 0    | 1    | X    | 0    | 0    | 1    | 0    | 1    |

X: don't care

Correspondence between the DCRAM address and the DCRAM data

| DCRAM address                               | DCRAM data                           | DCRAM address                                | DCRAM data                             |
|---|--------------------------------------|--|--|
| DA0 <sub>1</sub> to DA5 <sub>1</sub>        | AC0 <sub>1</sub> to AC7 <sub>1</sub> | (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 8  | AC0 <sub>9</sub> to AC7 <sub>9</sub>   |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 1 | AC0 <sub>2</sub> to AC7 <sub>2</sub> | (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 9  | AC0 <sub>10</sub> to AC7 <sub>10</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 2 | AC0 <sub>3</sub> to AC7 <sub>3</sub> | (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 10 | AC0 <sub>11</sub> to AC7 <sub>11</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 3 | AC0 <sub>4</sub> to AC7 <sub>4</sub> | (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 11 | AC0 <sub>12</sub> to AC7 <sub>12</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 4 | AC0 <sub>5</sub> to AC7 <sub>5</sub> | (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 12 | AC0 <sub>13</sub> to AC7 <sub>13</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 5 | AC0 <sub>6</sub> to AC7 <sub>6</sub> | (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 13 | AC0 <sub>14</sub> to AC7 <sub>14</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 6 | AC0 <sub>7</sub> to AC7 <sub>7</sub> | (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 14 | AC0 <sub>15</sub> to AC7 <sub>15</sub> |
| (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 7 | AC0 <sub>8</sub> to AC7 <sub>8</sub> | (DA0 <sub>1</sub> to DA5 <sub>1</sub> ) + 15 | AC0 <sub>16</sub> to AC7 <sub>16</sub> |

## LC75810E/T

• ALATCH data write …… <Write data to the ALATCH>

| Code |     |     |     |     |     |     |     |     |      |      |      |      |      |      |      |
|------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|
| D56  | D57 | D58 | D59 | D60 | D61 | D62 | D63 | D64 | D65  | D66  | D67  | D68  | D69  | D70  | D71  |
| AD1  | AD2 | AD3 | AD4 | AD5 | AD6 | AD7 | AD8 | AD9 | AD10 | AD11 | AD12 | AD13 | AD14 | AD15 | AD16 |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D72  | D73  | D74  | D75  | D76  | D77  | D78  | D79  | D80  | D81  | D82  | D83  | D84  | D85  | D86  | D87  |
| AD17 | AD18 | AD19 | AD20 | AD21 | AD22 | AD23 | AD24 | AD25 | AD26 | AD27 | AD28 | AD29 | AD30 | AD31 | AD32 |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D88  | D89  | D90  | D91  | D92  | D93  | D94  | D95  | D96  | D97  | D98  | D99  | D100 | D101 | D102 | D103 |
| AD33 | AD34 | AD35 | AD36 | AD37 | AD38 | AD39 | AD40 | AD41 | AD42 | AD43 | AD44 | AD45 | AD46 | AD47 | AD48 |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D104 | D105 | D106 | D107 | D108 | D109 | D110 | D111 | D112 | D113 | D114 | D115 | D116 | D117 | D118 | D119 |
| AD49 | AD50 | AD51 | AD52 | AD53 | AD54 | AD55 | AD56 | AD57 | AD58 | AD59 | AD60 | AD61 | AD62 | AD63 | AD64 |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D120 | D121 | D122 | D123 | D124 | D125 | D126 | D127 | D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 |
| AD65 | AD66 | AD67 | AD68 | AD69 | AD70 | AD71 | AD72 | AD73 | AD74 | AD75 | AD76 | AD77 | AD78 | AD79 | AD80 |

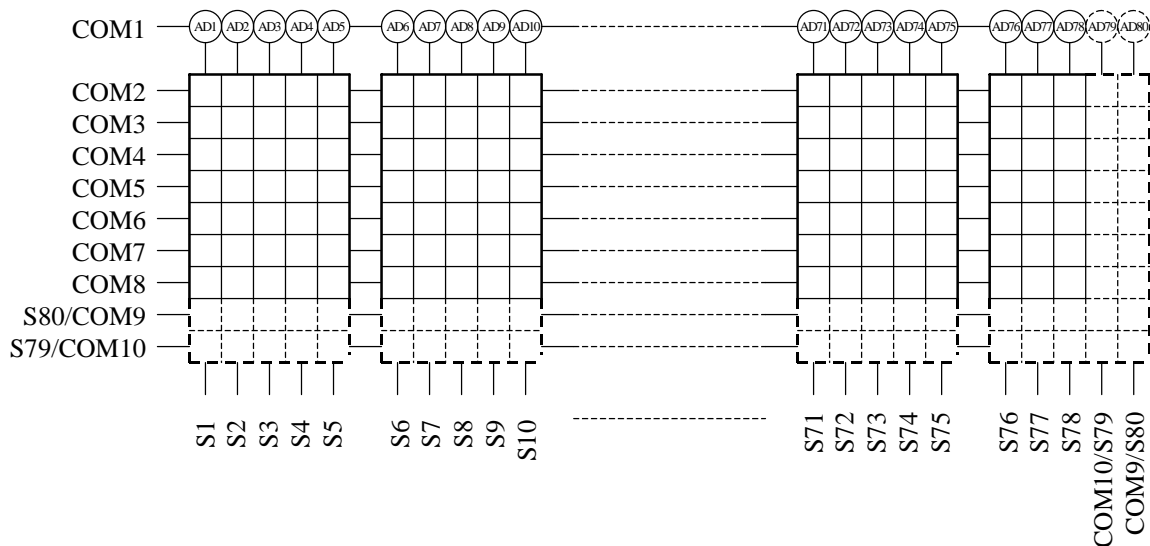
| Code |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| X    | X    | X    | 0    | 0    | 1    | 1    | 0    |

X: don't care

**AD1 to AD80: ADATA display data**

In addition to the 5 × 7, 5 × 8, 5 × 9, 6 × 7, 6 × 8, or 6 × 9 dot matrix display data (MDATA), the LC75810E/T also supports an accessory display of 5 or 6 segments (ADATA) at each display digit, and allows arbitrary data to be displayed directly without going through CGROM or CGRAM. The figure below shows the correspondence between that data and the display. When AD<sub>n</sub> = 1 (where n is an integer between 1 and 80), the segment corresponding to that data will be turned on.

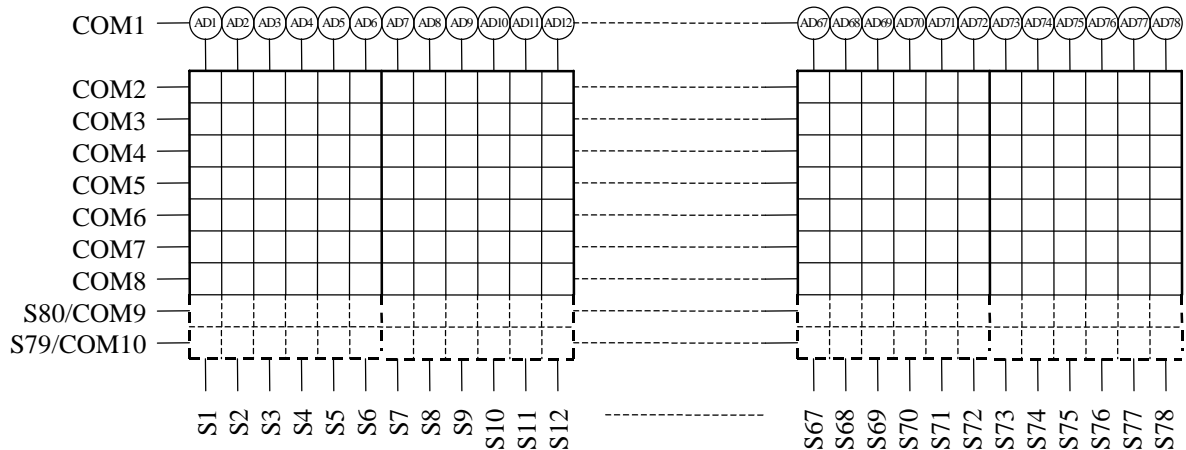
**5-dot font width (5 × 7, 5 × 8, or 5 × 9 dots)**





## LC75810E/T

6-dot font width (6 × 7, 6 × 8, or 6 × 9 dots)



Correspondence between ADATA and the output pins

| ADATA | Corresponding output pin |
|-------|--------------------------|
| AD1   | S1                       |
| AD2   | S2                       |
| AD3   | S3                       |
| AD4   | S4                       |
| AD5   | S5                       |
| AD6   | S6                       |
| AD7   | S7                       |
| AD8   | S8                       |
| AD9   | S9                       |
| AD10  | S10                      |
| AD11  | S11                      |
| AD12  | S12                      |
| AD13  | S13                      |
| AD14  | S14                      |
| AD15  | S15                      |
| AD16  | S16                      |
| AD17  | S17                      |
| AD18  | S18                      |
| AD19  | S19                      |
| AD20  | S20                      |
| AD21  | S21                      |
| AD22  | S22                      |
| AD23  | S23                      |
| AD24  | S24                      |
| AD25  | S25                      |
| AD26  | S26                      |
| AD27  | S27                      |
| AD28  | S28                      |
| AD29  | S29                      |
| AD30  | S30                      |

| ADATA | Corresponding output pin |
|-------|--------------------------|
| AD31  | S31                      |
| AD32  | S32                      |
| AD33  | S33                      |
| AD34  | S34                      |
| AD35  | S35                      |
| AD36  | S36                      |
| AD37  | S37                      |
| AD38  | S38                      |
| AD39  | S39                      |
| AD40  | S40                      |
| AD41  | S41                      |
| AD42  | S42                      |
| AD43  | S43                      |
| AD44  | S44                      |
| AD45  | S45                      |
| AD46  | S46                      |
| AD47  | S47                      |
| AD48  | S48                      |
| AD49  | S49                      |
| AD50  | S50                      |
| AD51  | S51                      |
| AD52  | S52                      |
| AD53  | S53                      |
| AD54  | S54                      |
| AD55  | S55                      |
| AD56  | S56                      |
| AD57  | S57                      |
| AD58  | S58                      |
| AD59  | S59                      |
| AD60  | S60                      |

| ADATA | Corresponding output pin |
|-------|--------------------------|
| AD61  | S61                      |
| AD62  | S62                      |
| AD63  | S63                      |
| AD64  | S64                      |
| AD65  | S65                      |
| AD66  | S66                      |
| AD67  | S67                      |
| AD68  | S68                      |
| AD69  | S69                      |
| AD70  | S70                      |
| AD71  | S71                      |
| AD72  | S72                      |
| AD73  | S73                      |
| AD74  | S74                      |
| AD75  | S75                      |
| AD76  | S76                      |
| AD77  | S77                      |
| AD78  | S78                      |
| AD79  | S79                      |
| AD80  | S80                      |

## LC75810E/T

• CGRAM data write ..... <Specifies the CGRAM address and stores data at that address.>

|      |     |     |     |     |     |     |     |     |      |      |      |      |      |      |      |
|------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|
| Code |     |     |     |     |     |     |     |     |      |      |      |      |      |      |      |
| D80  | D81 | D82 | D83 | D84 | D85 | D86 | D87 | D88 | D89  | D90  | D91  | D92  | D93  | D94  | D95  |
| CD1  | CD2 | CD3 | CD4 | CD5 | CD6 | CD7 | CD8 | CD9 | CD10 | CD11 | CD12 | CD13 | CD14 | CD15 | CD16 |

|      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| D96  | D97  | D98  | D99  | D100 | D101 | D102 | D103 | D104 | D105 | D106 | D107 | D108 | D109 | D110 | D111 |
| CD17 | CD18 | CD19 | CD20 | CD21 | CD22 | CD23 | CD24 | CD25 | CD26 | CD27 | CD28 | CD29 | CD30 | CD31 | CD32 |

|      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| D112 | D113 | D114 | D115 | D116 | D117 | D118 | D119 | D120 | D121 | D122 | D123 | D124 | D125 | D126 | D127 |
| CD33 | CD34 | CD35 | CD36 | CD37 | CD38 | CD39 | CD40 | CD41 | CD42 | CD43 | CD44 | CD45 | X    | X    | X    |

|      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| CA0  | CA1  | CA2  | CA3  | CA4  | CA5  | CA6  | CA7  | WM   | X    | X    | 0    | 0    | 1    | 1    | 1    |

X: don't care

CA0 to CA7: CGRAM address

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 |
|-----|-----|-----|-----|-----|-----|-----|-----|

|                       |  |                      |
|-----------------------|--|----------------------|
| LSB                   |  | MSB                  |
| ↑                     |  | ↑                    |
| Least significant bit |  | Most significant bit |

CD1 to CD45: CGRAM data ( $5 \times 7$ ,  $5 \times 8$ , or  $5 \times 9$  dot matrix display data)

The bit CDn (where n is an integer between 1 and 45) corresponds to the  $5 \times 7$ ,  $5 \times 8$ , or  $5 \times 9$  dot matrix display data. The figure below shows that correspondence. When CDn is 1, the dots which correspond to that data will be turned on.

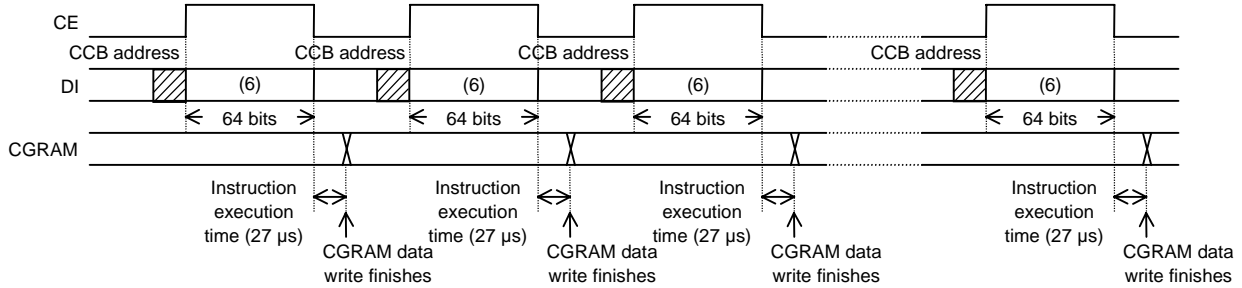
|      |      |      |      |      |
|------|------|------|------|------|
| CD1  | CD2  | CD3  | CD4  | CD5  |
| CD6  | CD7  | CD8  | CD9  | CD10 |
| CD11 | CD12 | CD13 | CD14 | CD15 |
| CD16 | CD17 | CD18 | CD19 | CD20 |
| CD21 | CD22 | CD23 | CD24 | CD25 |
| CD26 | CD27 | CD28 | CD29 | CD30 |
| CD31 | CD32 | CD33 | CD34 | CD35 |
| CD36 | CD37 | CD38 | CD39 | CD40 |
| CD41 | CD42 | CD43 | CD44 | CD45 |

\*22: CD1 to CD35:  $5 \times 7$  dot matrix display data  
 CD1 to CD40:  $5 \times 8$  dot matrix display data  
 CD1 to CD45:  $5 \times 9$  dot matrix display data

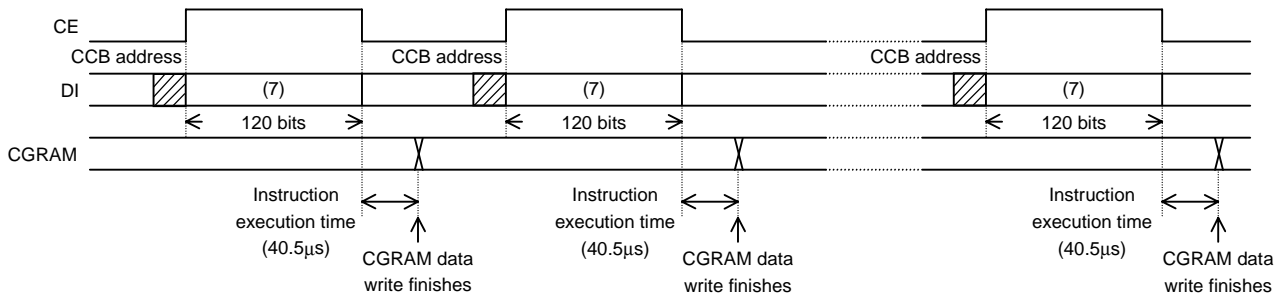
WM: Sets the method of writing data to CGRAM.

| WM | CGRAM data write method  |
|----|--|
| 0  | Normal CGRAM data write (Specifies a CGRAM address and write a CGRAM data.)                                      |
| 1  | Double write mode CGRAM data write (Specifies two CGRAM addresses and writes two CGRAM data to those addresses.) |

\*23: • CGRAM data write method when WM is 0.



• CGRAM data write method when WM is 1.



Note that the instruction execution times of 27 μs and 40.5 μs apply when fosc = 300 kHz, and that these times will differ when the oscillator frequency fosc differs.

Data format (6) (64 bits)

| Code |     |     |     |     |     |     |     |     |      |      |      |      |      |      |      |
|------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|
| D80  | D81 | D82 | D83 | D84 | D85 | D86 | D87 | D88 | D89  | D90  | D91  | D92  | D93  | D94  | D95  |
| CD1  | CD2 | CD3 | CD4 | CD5 | CD6 | CD7 | CD8 | CD9 | CD10 | CD11 | CD12 | CD13 | CD14 | CD15 | CD16 |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D96  | D97  | D98  | D99  | D100 | D101 | D102 | D103 | D104 | D105 | D106 | D107 | D108 | D109 | D110 | D111 |
| CD17 | CD18 | CD19 | CD20 | CD21 | CD22 | CD23 | CD24 | CD25 | CD26 | CD27 | CD28 | CD29 | CD30 | CD31 | CD32 |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D112 | D113 | D114 | D115 | D116 | D117 | D118 | D119 | D120 | D121 | D122 | D123 | D124 | D125 | D126 | D127 |
| CD33 | CD34 | CD35 | CD36 | CD37 | CD38 | CD39 | CD40 | CD41 | CD42 | CD43 | CD44 | CD45 | X    | X    | X    |

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| CA0  | CA1  | CA2  | CA3  | CA4  | CA5  | CA6  | CA7  | 0    | X    | X    | 0    | 0    | 1    | 1    | 1    |

X: don't care

## LC75810E/T

### Data format (7) (120 bits)

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                   |                   |                   |                   |                   |                   |                   |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D24              | D25              | D26              | D27              | D28              | D29              | D30              | D31              | D32              | D33               | D34               | D35               | D36               | D37               | D38               | D39               |
| CD1 <sub>1</sub> | CD2 <sub>1</sub> | CD3 <sub>1</sub> | CD4 <sub>1</sub> | CD5 <sub>1</sub> | CD6 <sub>1</sub> | CD7 <sub>1</sub> | CD8 <sub>1</sub> | CD9 <sub>1</sub> | CD10 <sub>1</sub> | CD11 <sub>1</sub> | CD12 <sub>1</sub> | CD13 <sub>1</sub> | CD14 <sub>1</sub> | CD15 <sub>1</sub> | CD16 <sub>1</sub> |

| Code              |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D40               | D41               | D42               | D43               | D44               | D45               | D46               | D47               | D48               | D49               | D50               | D51               | D52               | D53               | D54               | D55               |
| CD17 <sub>1</sub> | CD18 <sub>1</sub> | CD19 <sub>1</sub> | CD20 <sub>1</sub> | CD21 <sub>1</sub> | CD22 <sub>1</sub> | CD23 <sub>1</sub> | CD24 <sub>1</sub> | CD25 <sub>1</sub> | CD26 <sub>1</sub> | CD27 <sub>1</sub> | CD28 <sub>1</sub> | CD29 <sub>1</sub> | CD30 <sub>1</sub> | CD31 <sub>1</sub> | CD32 <sub>1</sub> |

| Code              |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |     |     |     |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-----|-----|-----|
| D56               | D57               | D58               | D59               | D60               | D61               | D62               | D63               | D64               | D65               | D66               | D67               | D68               | D69 | D70 | D71 |
| CD33 <sub>1</sub> | CD34 <sub>1</sub> | CD35 <sub>1</sub> | CD36 <sub>1</sub> | CD37 <sub>1</sub> | CD38 <sub>1</sub> | CD39 <sub>1</sub> | CD40 <sub>1</sub> | CD41 <sub>1</sub> | CD42 <sub>1</sub> | CD43 <sub>1</sub> | CD44 <sub>1</sub> | CD45 <sub>1</sub> | X   | X   | X   |

| Code             |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D72              | D73              | D74              | D75              | D76              | D77              | D78              | D79              | D80              | D81              | D82              | D83              | D84              | D85              | D86              | D87              |
| CA0 <sub>1</sub> | CA1 <sub>1</sub> | CA2 <sub>1</sub> | CA3 <sub>1</sub> | CA4 <sub>1</sub> | CA5 <sub>1</sub> | CA6 <sub>1</sub> | CA7 <sub>1</sub> | CD1 <sub>2</sub> | CD2 <sub>2</sub> | CD3 <sub>2</sub> | CD4 <sub>2</sub> | CD5 <sub>2</sub> | CD6 <sub>2</sub> | CD7 <sub>2</sub> | CD8 <sub>2</sub> |

| Code             |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D88              | D89               | D90               | D91               | D92               | D93               | D94               | D95               | D96               | D97               | D98               | D99               | D100              | D101              | D102              | D103              |
| CD9 <sub>2</sub> | CD10 <sub>2</sub> | CD11 <sub>2</sub> | CD12 <sub>2</sub> | CD13 <sub>2</sub> | CD14 <sub>2</sub> | CD15 <sub>2</sub> | CD16 <sub>2</sub> | CD17 <sub>2</sub> | CD18 <sub>2</sub> | CD19 <sub>2</sub> | CD20 <sub>2</sub> | CD21 <sub>2</sub> | CD22 <sub>2</sub> | CD23 <sub>2</sub> | CD24 <sub>2</sub> |

| Code              |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D104              | D105              | D106              | D107              | D108              | D109              | D110              | D111              | D112              | D113              | D114              | D115              | D116              | D117              | D118              | D119              |
| CD25 <sub>2</sub> | CD26 <sub>2</sub> | CD27 <sub>2</sub> | CD28 <sub>2</sub> | CD29 <sub>2</sub> | CD30 <sub>2</sub> | CD31 <sub>2</sub> | CD32 <sub>2</sub> | CD33 <sub>2</sub> | CD34 <sub>2</sub> | CD35 <sub>2</sub> | CD36 <sub>2</sub> | CD37 <sub>2</sub> | CD38 <sub>2</sub> | CD39 <sub>2</sub> | CD40 <sub>2</sub> |

| Code              |                   |                   |                   |                   |      |      |      |                  |                  |                  |                  |                  |                  |                  |                  |
|-------------------|-------------------|-------------------|-------------------|-------------------|------|------|------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D120              | D121              | D122              | D123              | D124              | D125 | D126 | D127 | D128             | D129             | D130             | D131             | D132             | D133             | D134             | D135             |
| CD41 <sub>2</sub> | CD42 <sub>2</sub> | CD43 <sub>2</sub> | CD44 <sub>2</sub> | CD45 <sub>2</sub> | X    | X    | X    | CA0 <sub>2</sub> | CA1 <sub>2</sub> | CA2 <sub>2</sub> | CA3 <sub>2</sub> | CA4 <sub>2</sub> | CA5 <sub>2</sub> | CA6 <sub>2</sub> | CA7 <sub>2</sub> |

| Code |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| 1    | X    | X    | 0    | 0    | 1    | 1    | 1    |

X: don't care

### Correspondence between the CGRAM address and the CGRAM data

|                                      |                                       |
|--------------------------------------|---------------------------------------|
| CGRAM address                        | CGRAM data                            |
| CA0 <sub>1</sub> to CA7 <sub>1</sub> | CD1 <sub>1</sub> to CD45 <sub>1</sub> |
| CA0 <sub>2</sub> to CA7 <sub>2</sub> | CD1 <sub>2</sub> to CD45 <sub>2</sub> |

## LC75810E/T

- Set display contrast …… <Sets the display contrast.>

| Code |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| D128 | D129 | D130 | D131 | D132 | D133 | D134 | D135 | D136 | D137 | D138 | D139 | D140 | D141 | D142 | D143 |
| CT0  | CT1  | CT2  | CT3  | X    | X    | X    | X    | CTC  | X    | X    | 0    | 1    | 0    | 0    | 0    |

X: don't care

CT0 to CT3: Sets the display contrast (11 steps)

| CT0 | CT1 | CT2 | CT3 | LCD drive 4/4 bias voltage supply $V_{LCD0}$ level |
|-----|-----|-----|-----|--|
| 0   | 0   | 0   | 0   | $0.94V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 2)$   |
| 1   | 0   | 0   | 0   | $0.91V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 3)$   |
| 0   | 1   | 0   | 0   | $0.88V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 4)$   |
| 1   | 1   | 0   | 0   | $0.85V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 5)$   |
| 0   | 0   | 1   | 0   | $0.82V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 6)$   |
| 1   | 0   | 1   | 0   | $0.79V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 7)$   |
| 0   | 1   | 1   | 0   | $0.76V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 8)$   |
| 1   | 1   | 1   | 0   | $0.73V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 9)$   |
| 0   | 0   | 0   | 1   | $0.70V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 10)$  |
| 1   | 0   | 0   | 1   | $0.67V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 11)$  |
| 0   | 1   | 0   | 1   | $0.64V_{LCD} = V_{LCD} - (0.03V_{LCD} \times 12)$  |

CTC: Sets the display contrast adjustment circuit state

| CTC | Display contrast adjustment circuit state   |
|-----|---|
| 0   | The display contrast adjustment circuit is disabled, and the $V_{LCD0}$ pin level is forced to the $V_{LCD}$ level. |
| 1   | The display contrast adjustment circuit operates, and the display contrast is adjusted.                             |

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it is also possible to be adjusted by varying the voltage level on the LCD driver block power supply  $V_{LCD}$  pin. However, the level on  $V_{LCD0}$  must be greater than or equal to 4.5V.

**Notes on the Power On and Power Off Sequences**

The following sequences must be observed when power is turned on and off. (See Figure 3.)

- At power on: Logic block power supply ( $V_{DD}$ ) on → LCD driver block power supply ( $V_{LCD}$ ) on.
- At power off: LCD driver block power supply ( $V_{LCD}$ ) off → Logic block power supply ( $V_{DD}$ ) off.

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

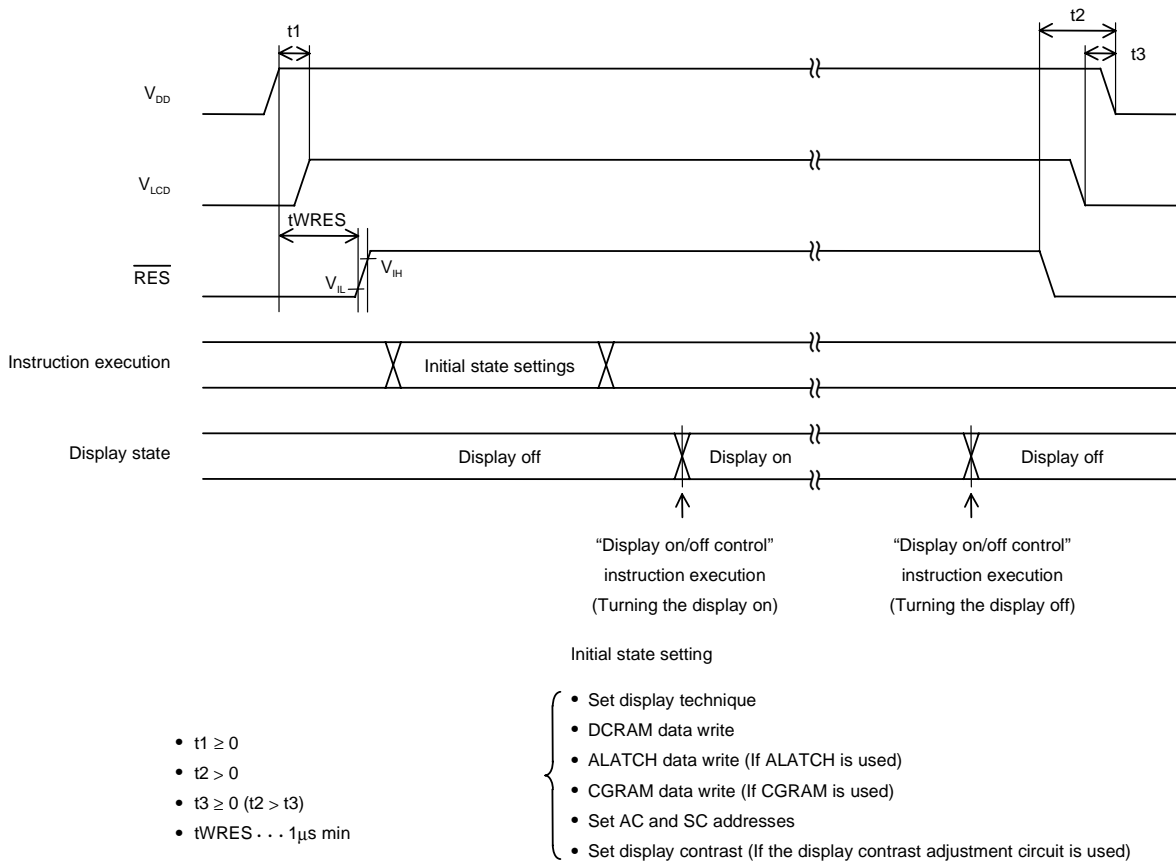
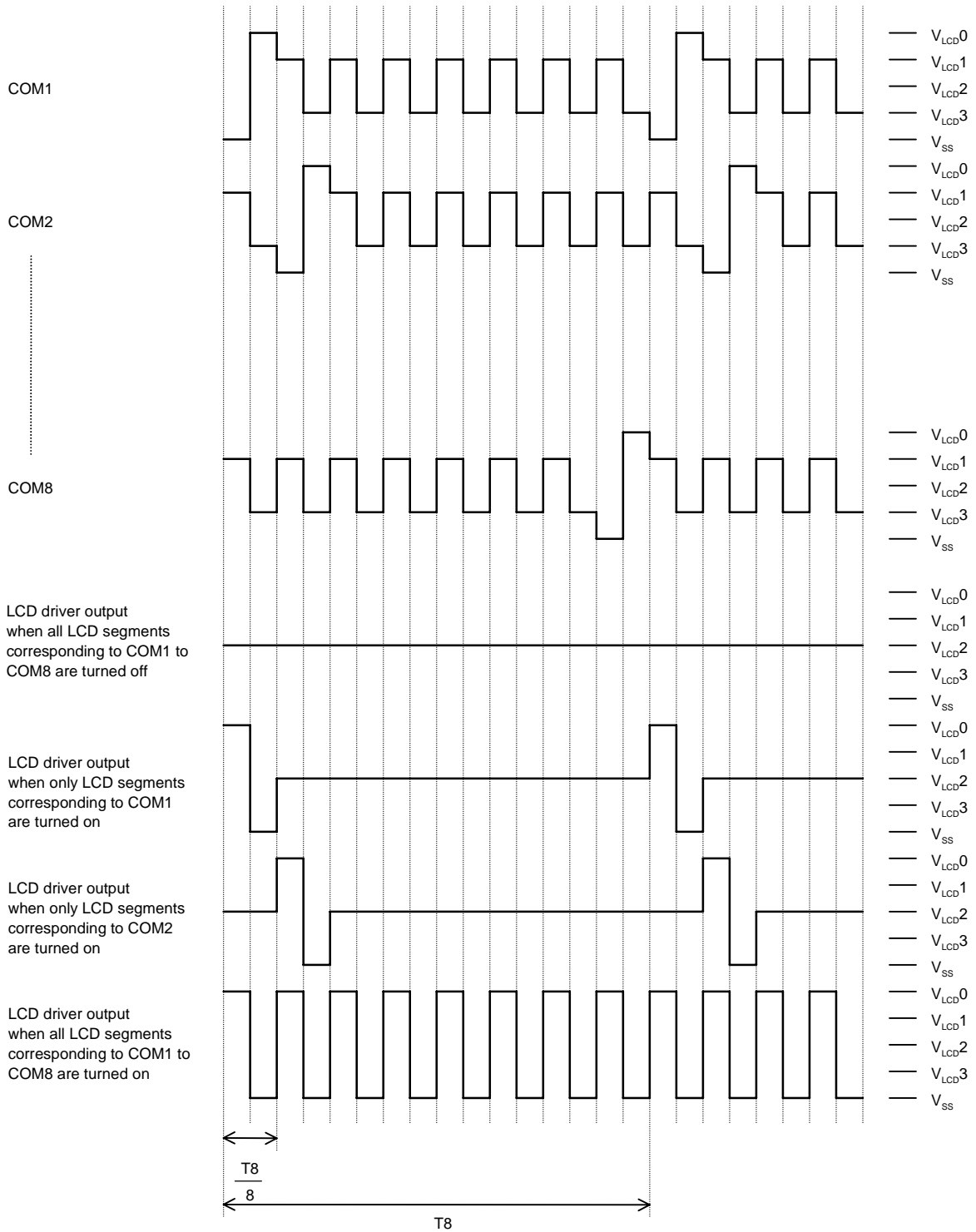


Figure 3

1/8 Duty, 1/4 Bias Drive Technique

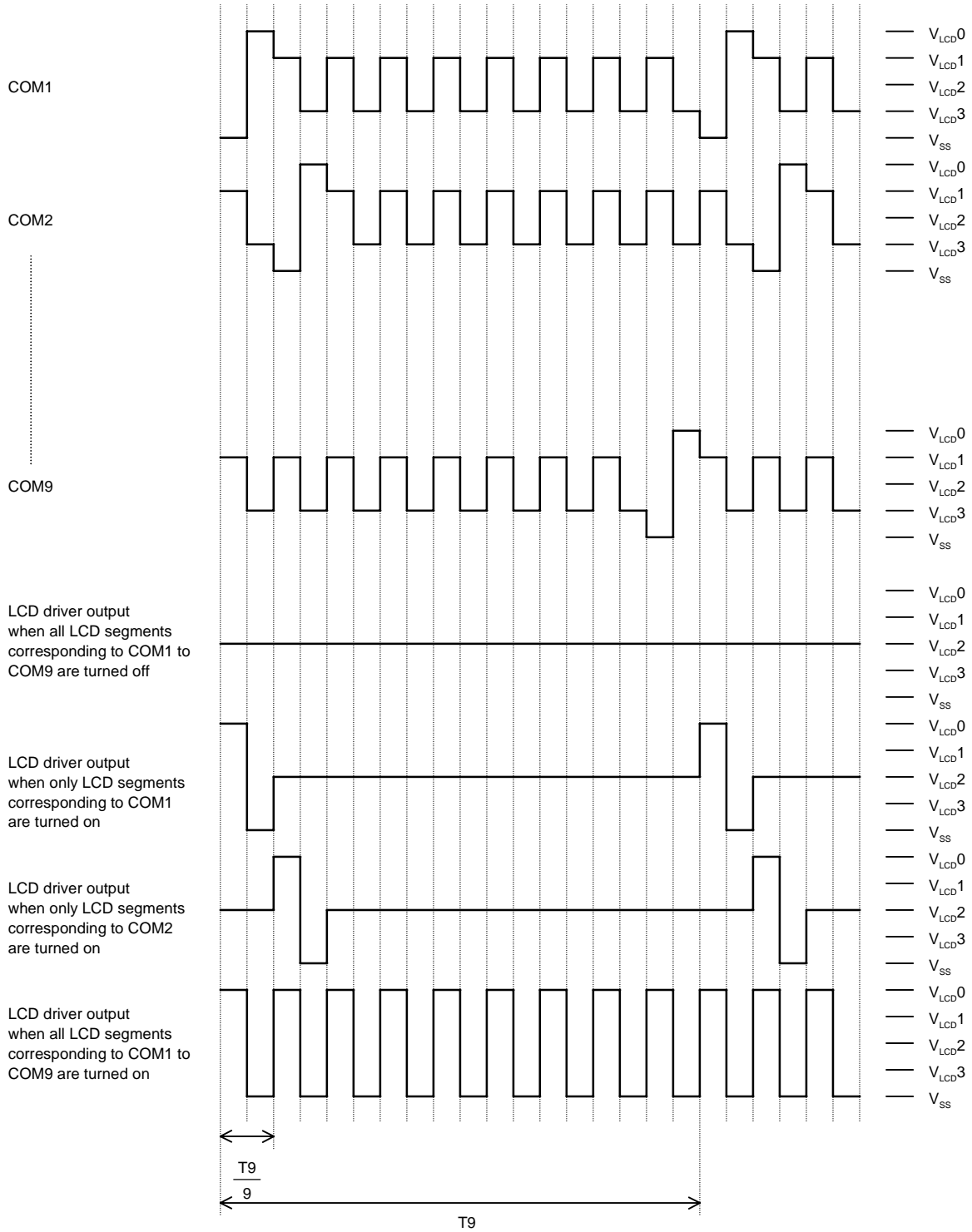


$$T8 = \frac{1}{f8}$$

When a "set display technique" instruction with FC = 0 is executed:  $f8 = \frac{fosc}{3072}$

When a "set display technique" instruction with FC = 1 is executed:  $f8 = \frac{fosc}{1536}$

1/9 Duty, 1/4 Bias Drive Technique



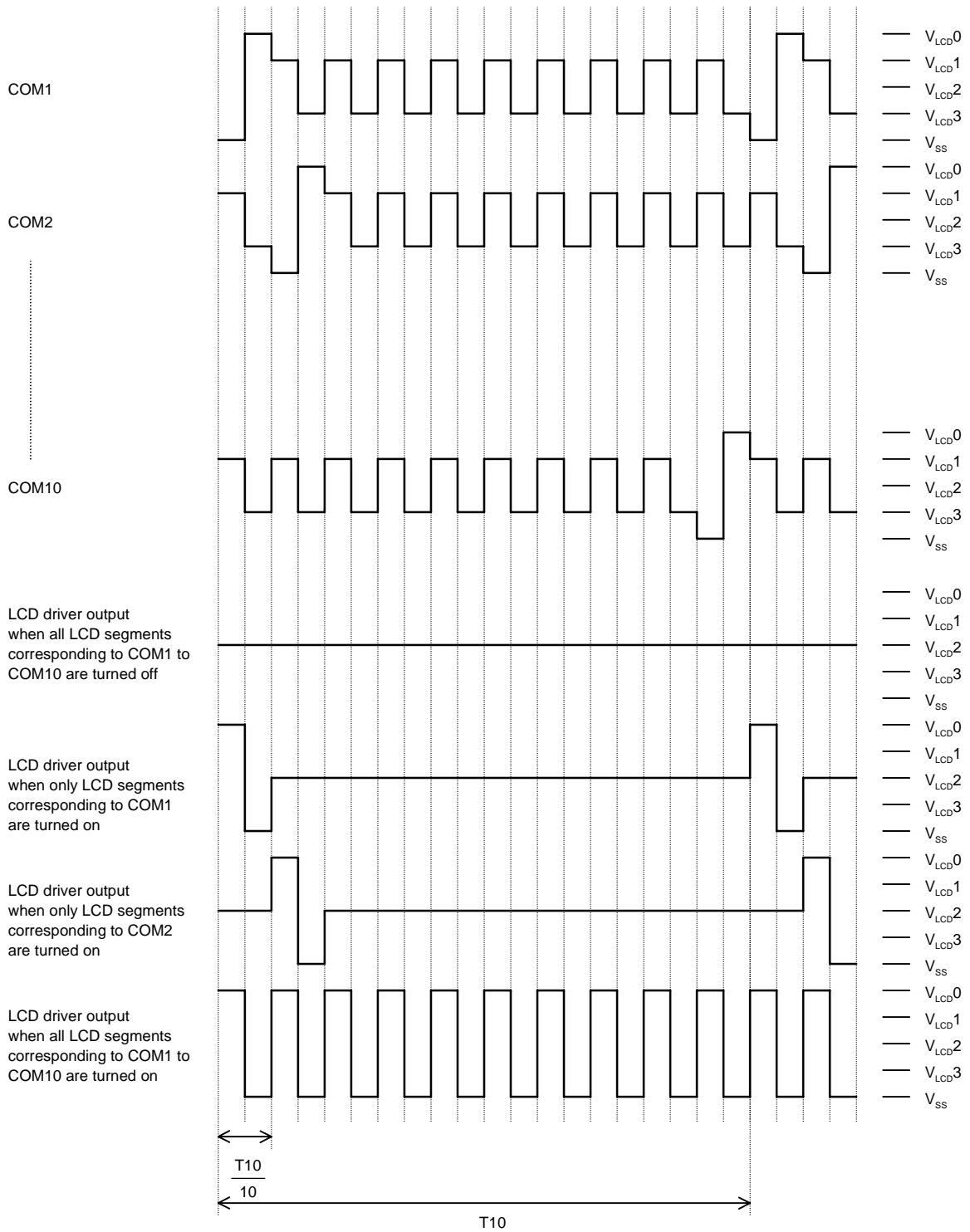
$$T_9 = \frac{1}{f_9}$$

When a "set display technique" instruction with FC = 0 is executed:  $f_9 = \frac{f_{osc}}{3456}$

When a "set display technique" instruction with FC = 1 is executed:  $f_9 = \frac{f_{osc}}{1728}$



1/10 Duty, 1/4 Bias Drive Technique



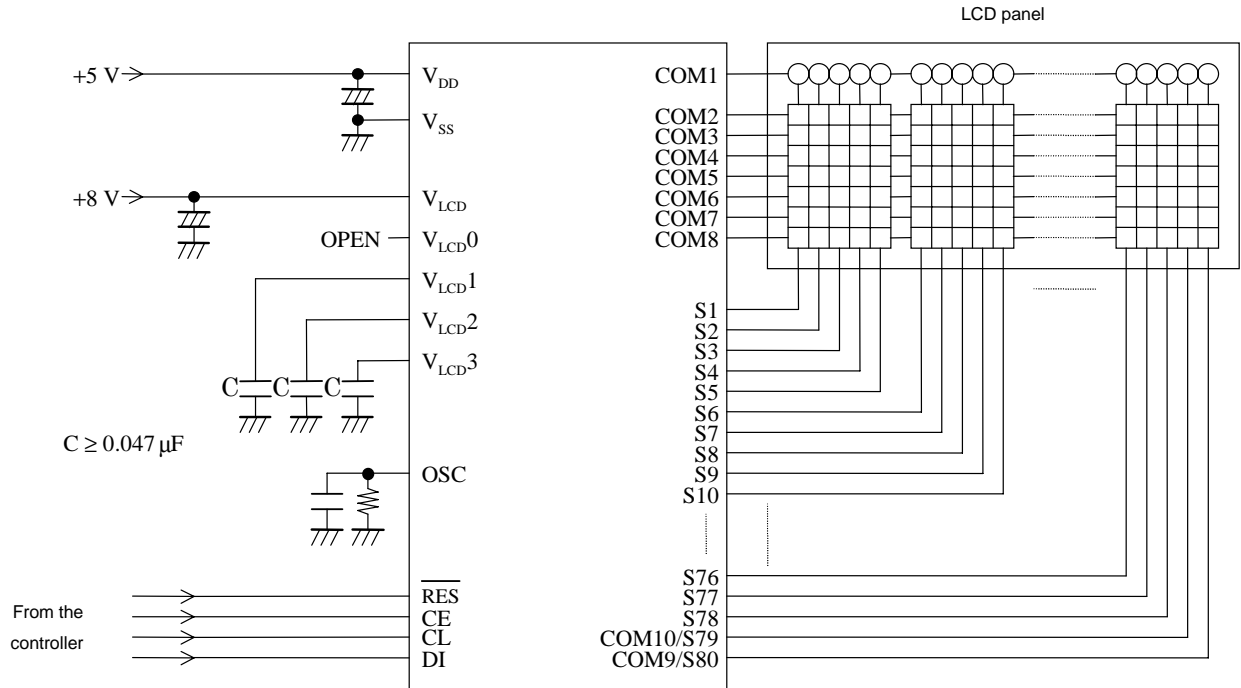
$$T_{10} = \frac{1}{f_{10}}$$

When a "set display technique" instruction with FC = 0 is executed:  $f_{10} = \frac{f_{osc}}{3840}$

When a "set display technique" instruction with FC = 1 is executed:  $f_{10} = \frac{f_{osc}}{1920}$

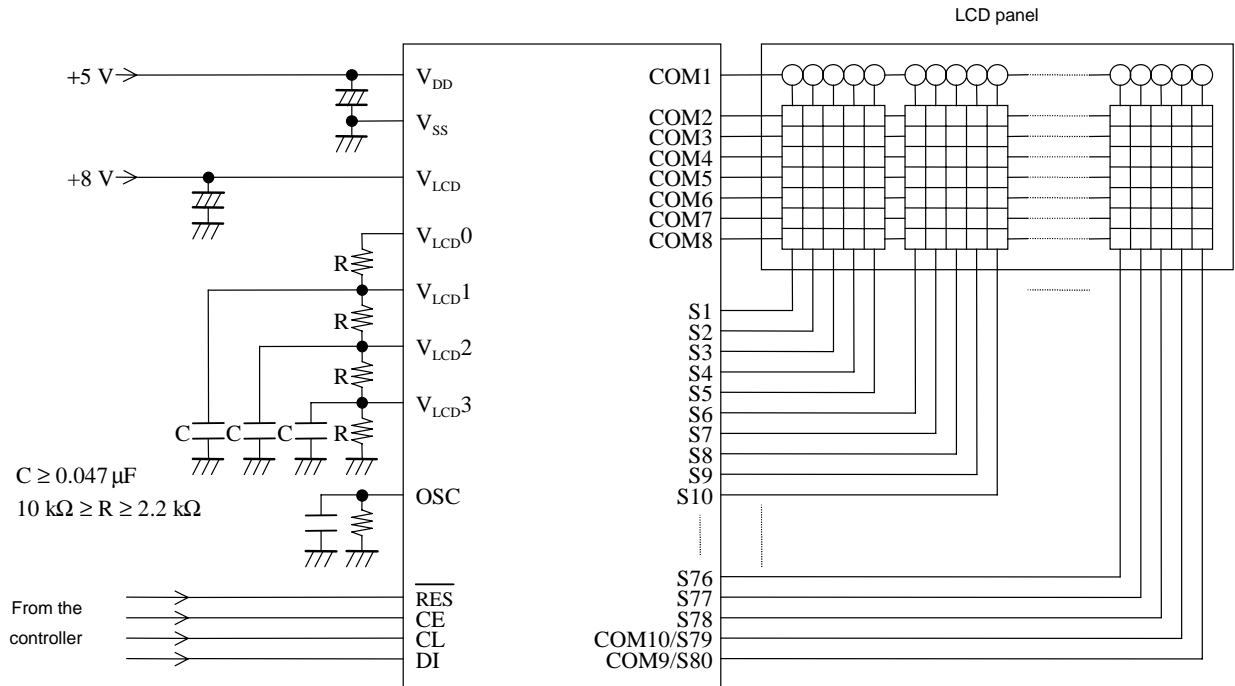
**Sample Application Circuit 1**

5 × 7 dot matrix, 1/8 duty, 1/4 bias drive (for use with normal panels)



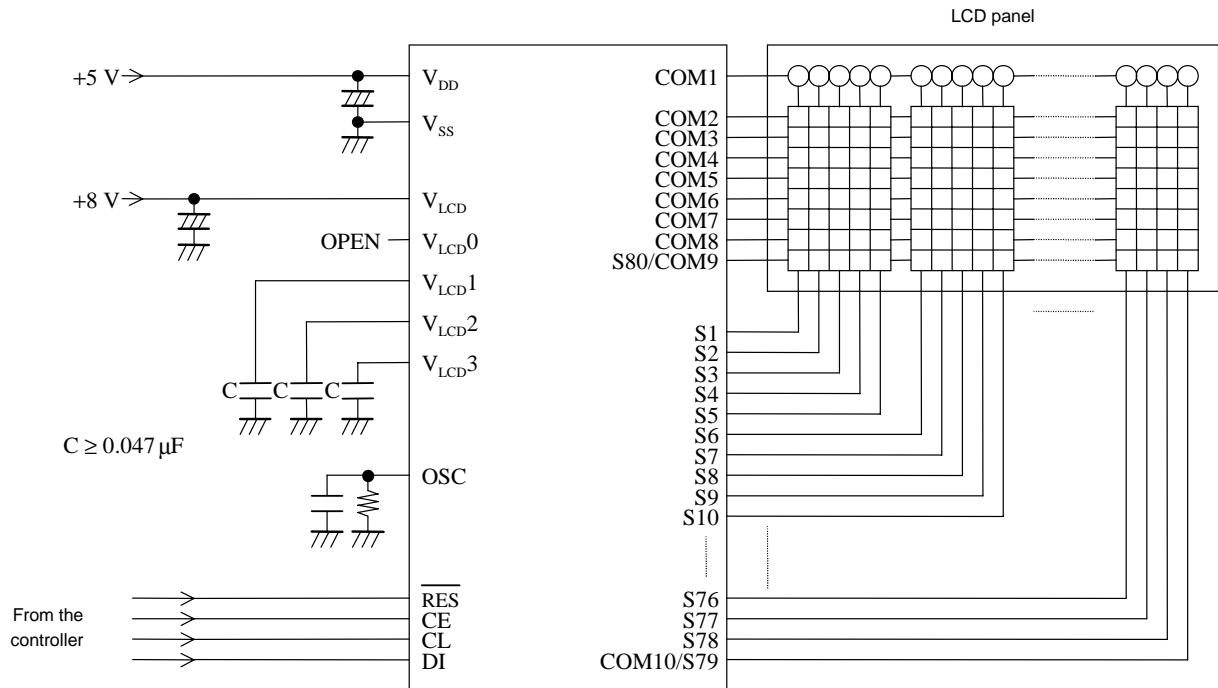
**Sample Application Circuit 2**

5 × 7 dot matrix, 1/8 duty, 1/4 bias drive (for use with large panels)



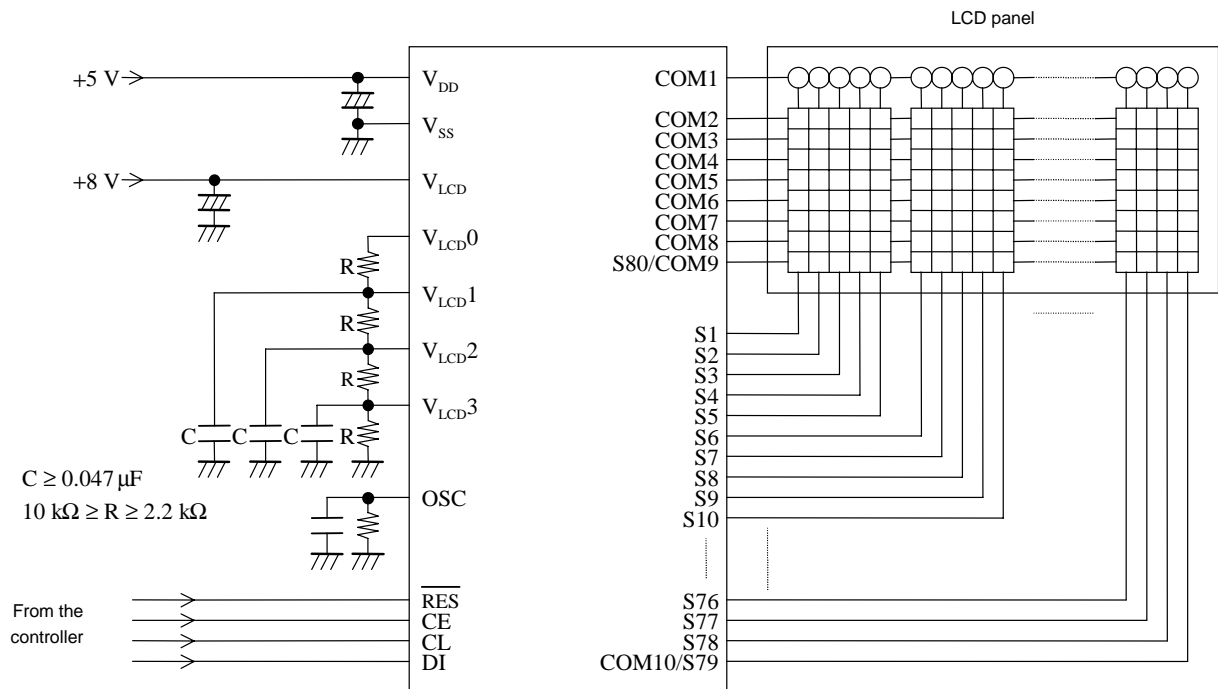
**Sample Application Circuit 3**

5 × 8 dot matrix, 1/9 duty, 1/4 bias drive (for use with normal panels)



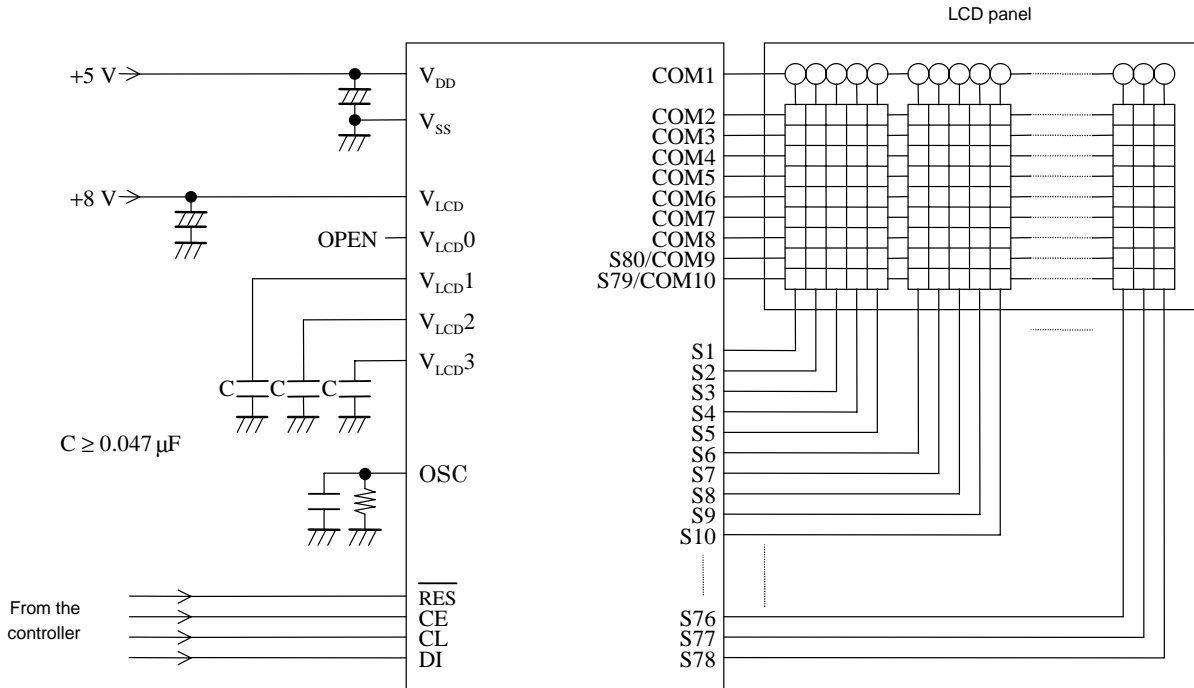
**Sample Application Circuit 4**

5 × 8 dot matrix, 1/9 duty, 1/4 bias drive (for use with large panels)



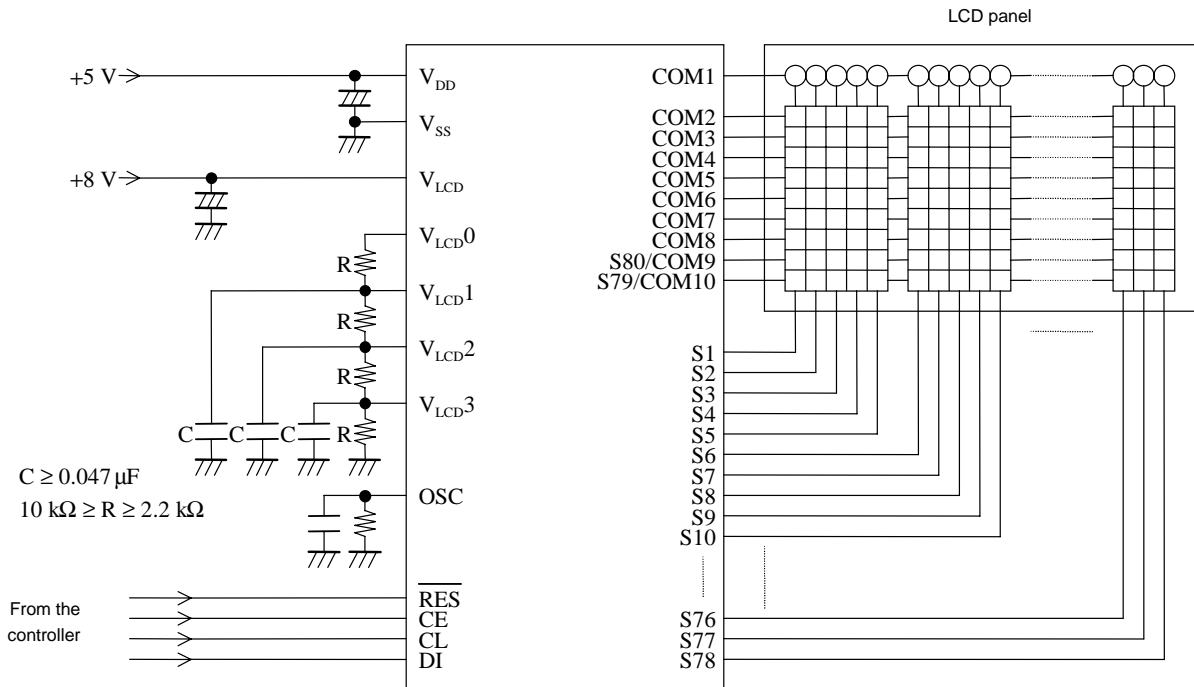
**Sample Application Circuit 5**

5 × 9 dot matrix, 1/10 duty, 1/4 bias drive (for use with normal panels)



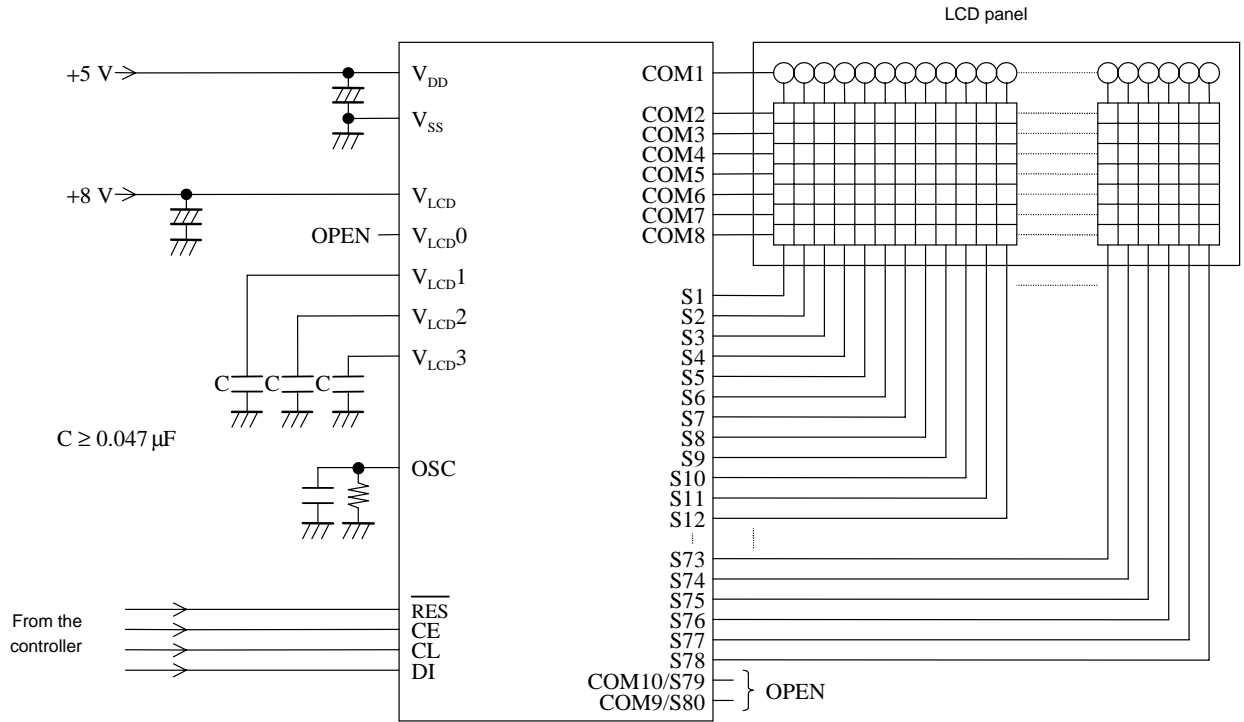
**Sample Application Circuit 6**

5 × 9 dot matrix, 1/10 duty, 1/4 bias drive (for use with large panels)



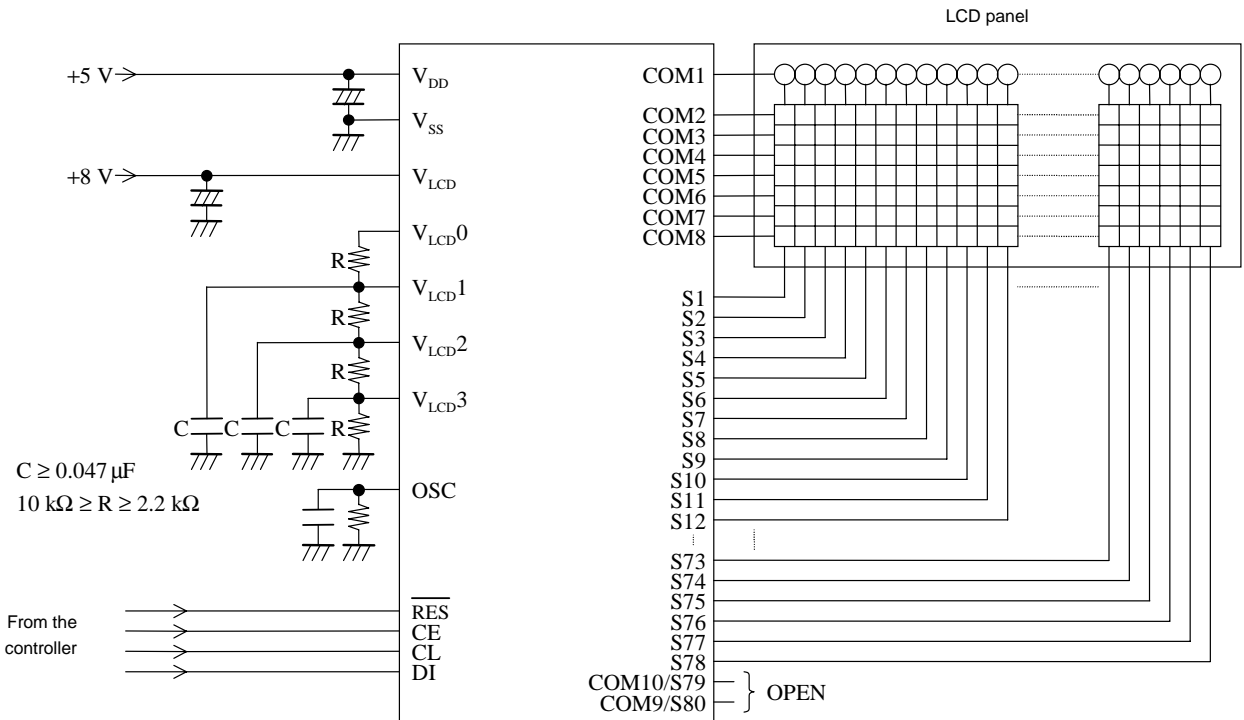
**Sample Application Circuit 7**

6 × 7 dot matrix, 1/8 duty, 1/4 bias drive (for use with normal panels)



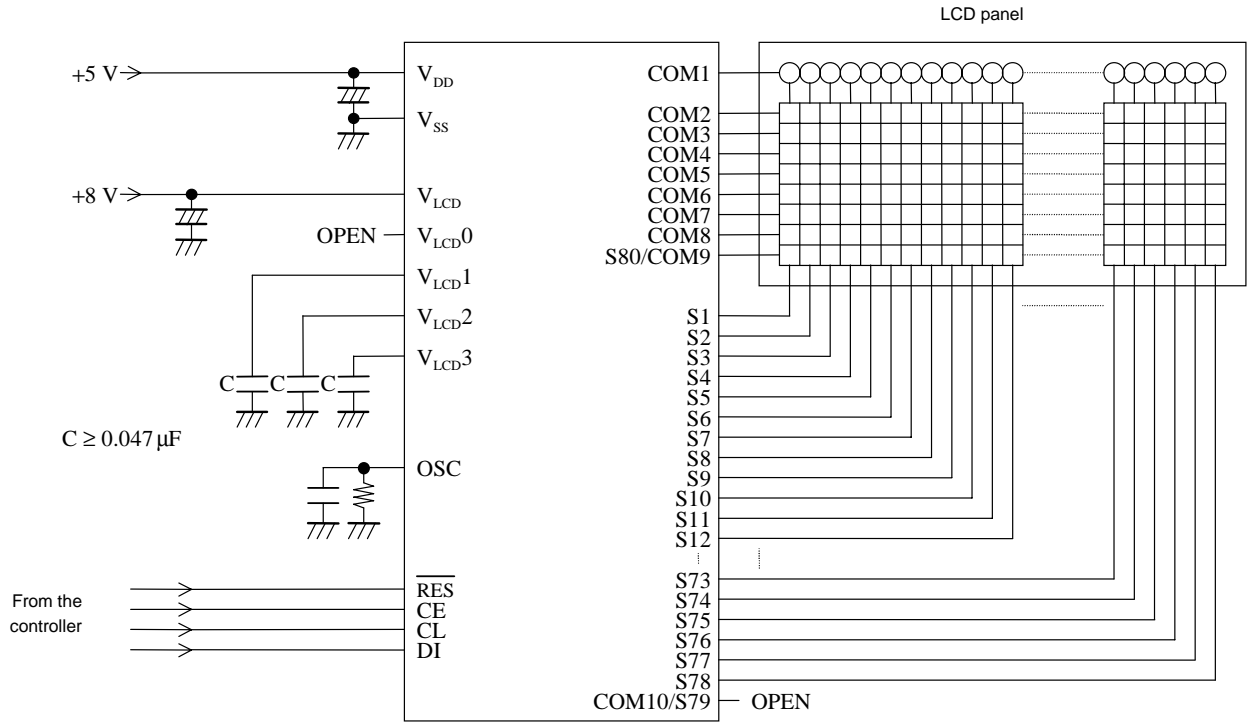
**Sample Application Circuit 8**

6 × 7 dot matrix, 1/8 duty, 1/4 bias drive (for use with large panels)



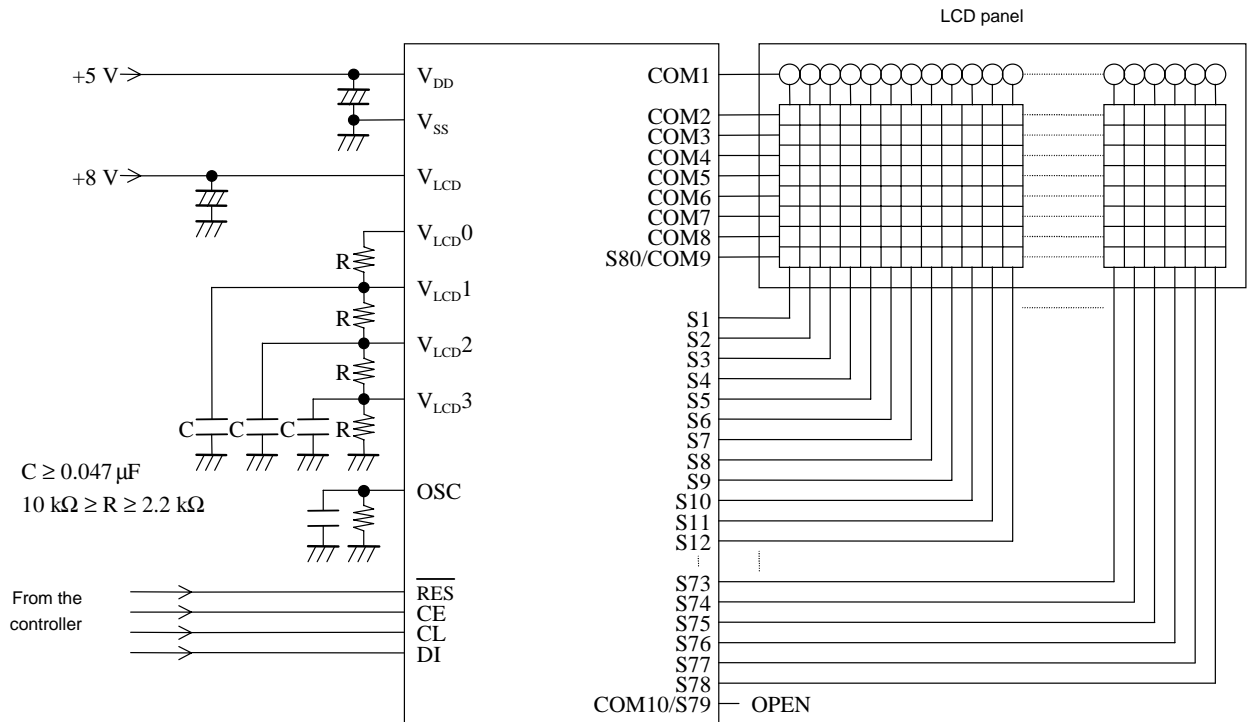
**Sample Application Circuit 9**

6 × 8 dot matrix, 1/9 duty, 1/4 bias drive (for use with normal panels)



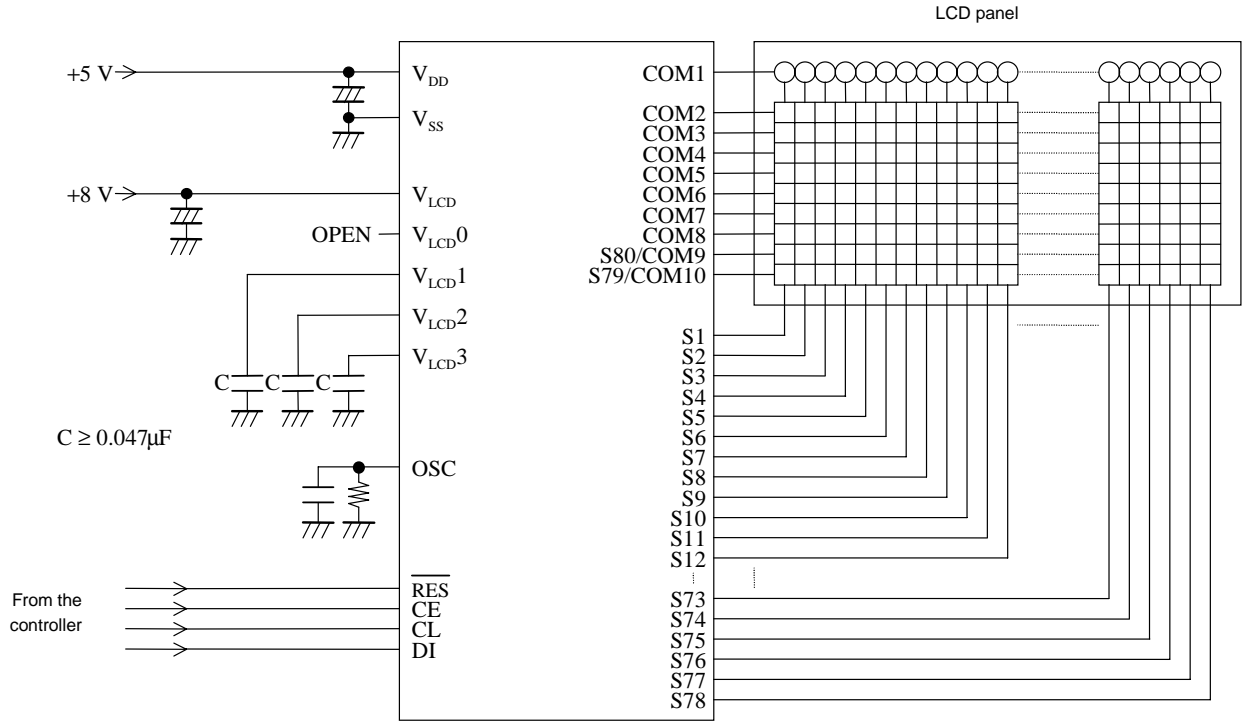
**Sample Application Circuit 10**

6 × 8 dot matrix, 1/9 duty, 1/4 bias drive (for use with large panels)



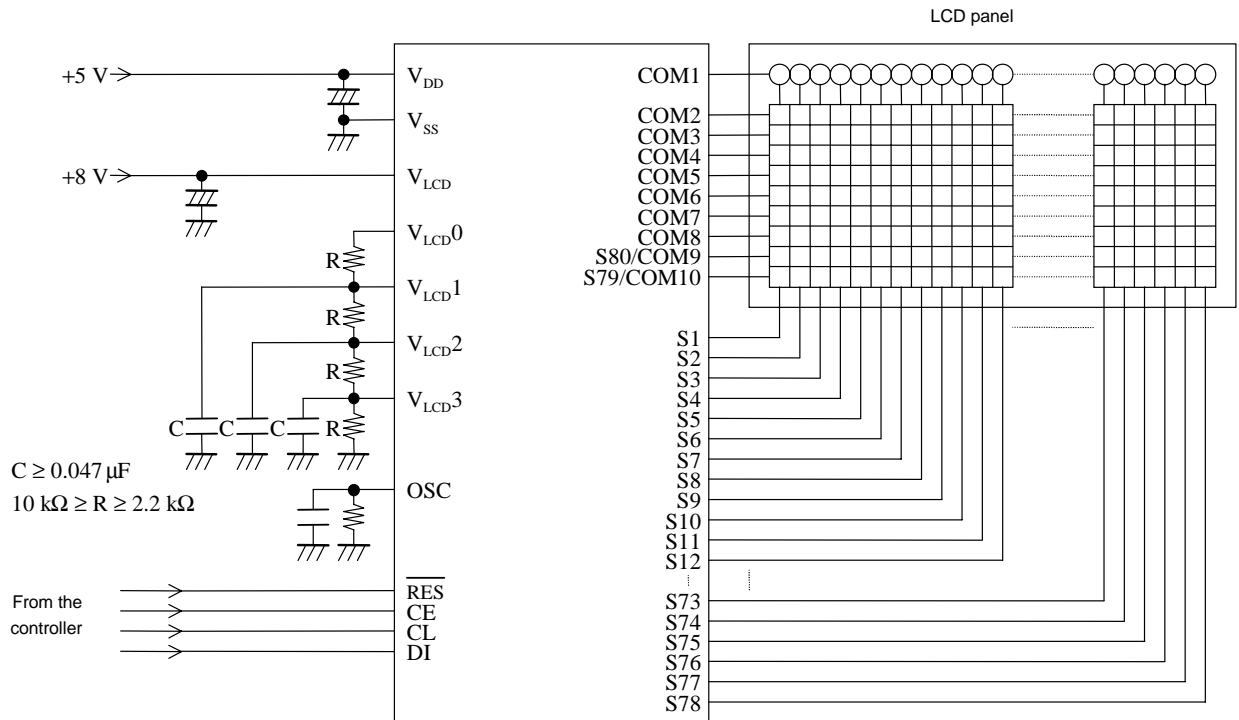
**Sample Application Circuit 11**

6 × 9 dot matrix, 1/10 duty, 1/4 bias drive (for use with normal panels)



**Sample Application Circuit 12**

6 × 9 dot matrix, 1/10 duty, 1/4 bias drive (for use with large panels)



Sample 1 showing the Correspondence between Instructions and the Display (Using the LC75810-8725 with a 5 x 7 dots, 16 digits x 1 line display)

| No. | LSB<br>D112 to D15 | Instruction (hexadecimal)   | MSB<br>D16 to D19 | Display | Operation   |
|-----|--------------------|---|-------------------|---------|---|
| 1   | D12 to D15         | Power application (initialization with the $\overline{\text{RES}}$ pin) | D16 to D19        |         | Initializes the IC.<br>The display is in the off state.   |
| 2   |                    | Set display technique   | 1 0 0 8           |         | Sets to the 1/8 duty 1/4 bias display technique, the 32 digits x 2 lines display structure, and the 5-dot font width at each digit. |
| 3   |                    | DCRAM data write (normal increment mode)                                | 3 5 0 1 A         |         | Writes the display data "S" to DCRAM address 00H.   |
| 4   |                    | DCRAM data write (normal increment mode)                                | 1 1 4             |         | Writes the display data "A" to DCRAM address 01H.   |
| 5   |                    | DCRAM data write (normal increment mode)                                | E 4               |         | Writes the display data "N" to DCRAM address 02H.   |
| 6   |                    | DCRAM data write (normal increment mode)                                | 9 5               |         | Writes the display data "Y" to DCRAM address 03H.   |
| 7   |                    | DCRAM data write (normal increment mode)                                | F 4               |         | Writes the display data "O" to DCRAM address 04H.   |
| 8   |                    | DCRAM data write (normal increment mode)                                | 0 2               |         | Writes the display data " " to DCRAM address 05H.   |
| 9   |                    | DCRAM data write (normal increment mode)                                | 9 4               |         | Writes the display data "I" to DCRAM address 06H.   |
| 10  |                    | DCRAM data write (normal increment mode)                                | 3 4               |         | Writes the display data "C" to DCRAM address 07H.   |
| 11  |                    | DCRAM data write (normal increment mode)                                | 0 2               |         | Writes the display data " " to DCRAM address 08H.   |
| 12  |                    | DCRAM data write (normal increment mode)                                | C 4               |         | Writes the display data "L" to DCRAM address 09H.   |
| 13  |                    | DCRAM data write (normal increment mode)                                | 3 4               |         | Writes the display data "C" to DCRAM address 0AH.   |
| 14  |                    | DCRAM data write (normal increment mode)                                | 7 3               |         | Writes the display data "7" to DCRAM address 0BH.   |
| 15  |                    | DCRAM data write (normal increment mode)                                | 5 3               |         | Writes the display data "5" to DCRAM address 0CH.   |
| 16  |                    | DCRAM data write (normal increment mode)                                | 8 3               |         | Writes the display data "8" to DCRAM address 0DH.   |
| 17  |                    | DCRAM data write (normal increment mode)                                | 1 3               |         | Writes the display data "1" to DCRAM address 0EH.   |

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| No. | Instruction (hexadecimal)                |           |          | MSB<br>D12 to D11 | Display | Operation   |
|-----|--|-----------|----------|-------------------|---------|---|
|     | LSB<br>D11 to D10                        | D10 to D7 | D6 to D4 |                   |         |   |
| 18  | DCRAM data write (normal increment mode) |           |          | 0 3               |         | Writes the display data "0" to DCRAM address 0FH. |
| 19  | DCRAM data write (normal increment mode) |           |          | 0 2               |         | Writes the display data " " to DCRAM address 10H. |
| 20  | DCRAM data write (normal increment mode) |           |          | C 4               |         | Writes the display data "L" to DCRAM address 11H. |
| 21  | DCRAM data write (normal increment mode) |           |          | 3 4               |         | Writes the display data "C" to DCRAM address 12H. |
| 22  | DCRAM data write (normal increment mode) |           |          | 4 4               |         | Writes the display data "D" to DCRAM address 13H. |
| 23  | DCRAM data write (normal increment mode) |           |          | 0 2               |         | Writes the display data " " to DCRAM address 14H. |
| 24  | DCRAM data write (normal increment mode) |           |          | 4 4               |         | Writes the display data "D" to DCRAM address 15H. |
| 25  | DCRAM data write (normal increment mode) |           |          | 2 5               |         | Writes the display data "R" to DCRAM address 16H. |
| 26  | DCRAM data write (normal increment mode) |           |          | 9 4               |         | Writes the display data "I" to DCRAM address 17H. |
| 27  | DCRAM data write (normal increment mode) |           |          | 6 5               |         | Writes the display data "V" to DCRAM address 18H. |
| 28  | DCRAM data write (normal increment mode) |           |          | 5 4               |         | Writes the display data "E" to DCRAM address 19H. |
| 29  | DCRAM data write (normal increment mode) |           |          | 2 5               |         | Writes the display data "R" to DCRAM address 1AH. |
| 30  | DCRAM data write (normal increment mode) |           |          | 0 2               |         | Writes the display data " " to DCRAM address 1BH. |
| 31  | DCRAM data write (normal increment mode) |           |          | 0 2               |         | Writes the display data " " to DCRAM address 1CH. |
| 32  | DCRAM data write (normal increment mode) |           |          | 0 2               |         | Writes the display data " " to DCRAM address 1DH. |
| 33  | DCRAM data write (normal increment mode) |           |          | 0 2               |         | Writes the display data " " to DCRAM address 1EH. |
| 34  | DCRAM data write (normal increment mode) |           |          | 0 2               |         | Writes the display data " " to DCRAM address 1FH. |

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| No. | Instruction (hexadecimal)                |           |          |          | MSB<br>D14 to D13 | Display | Operation  |
|-----|--|-----------|----------|----------|-------------------|---------|--|
|     | D15 to D11                               | D10 to D7 | D6 to D3 | D2 to D0 |                   |         |  |
| 35  | DCRAM data write (normal increment mode) |           |          |          | 4                 |         | Writes the display data "D" to DCRAM address 20H.  |
| 36  | DCRAM data write (normal increment mode) |           |          |          | F                 |         | Writes the display data "O" to DCRAM address 21H.  |
| 37  | DCRAM data write (normal increment mode) |           |          |          | 4                 |         | Writes the display data "T" to DCRAM address 22H.  |
| 38  | DCRAM data write (normal increment mode) |           |          |          | 0                 |         | Writes the display data " " to DCRAM address 23H.  |
| 39  | DCRAM data write (normal increment mode) |           |          |          | D                 |         | Writes the display data "M" to DCRAM address 24H.  |
| 40  | DCRAM data write (normal increment mode) |           |          |          | 1                 |         | Writes the display data "A" to DCRAM address 25H.  |
| 41  | DCRAM data write (normal increment mode) |           |          |          | 4                 |         | Writes the display data "T" to DCRAM address 26H.  |
| 42  | DCRAM data write (normal increment mode) |           |          |          | 2                 |         | Writes the display data "R" to DCRAM address 27H.  |
| 43  | DCRAM data write (normal increment mode) |           |          |          | 9                 |         | Writes the display data "I" to DCRAM address 28H.  |
| 44  | DCRAM data write (normal increment mode) |           |          |          | 8                 |         | Writes the display data "X" to DCRAM address 29H.  |
| 45  | DCRAM data write (normal increment mode) |           |          |          | 0                 |         | Writes the display data " " to DCRAM address 2AH.  |
| 46  | DCRAM data write (normal increment mode) |           |          |          | 4                 |         | Writes the display data "T" to DCRAM address 2BH.  |
| 47  | DCRAM data write (normal increment mode) |           |          |          | 9                 |         | Writes the display data "Y" to DCRAM address 2CH.  |
| 48  | DCRAM data write (normal increment mode) |           |          |          | 0                 |         | Writes the display data "P" to DCRAM address 2DH.  |
| 49  | DCRAM data write (normal increment mode) |           |          |          | 5                 |         | Writes the display data "E" to DCRAM address 2EH.  |
| 50  | DCRAM data write (normal increment mode) |           |          |          | 0                 |         | Writes the display data " " to DCRAM address 2FH.  |
| 51  | Set AC and SC addresses                  |           |          |          | 0                 |         | Sets AC to the DCRAM address 00H, SC to the horizontal dot address 0H and the vertical dot address 0H. |

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| No. | Instruction (hexadecimal) |              |              |              | MSB          |              |              |         | Operation   |
|-----|---------------------------|--------------|--------------|--------------|--------------|--------------|--------------|---------|---|
|     | LSB<br>D112 to D115       | D120 to D123 | D124 to D127 | D128 to D131 | D132 to D135 | D136 to D139 | D140 to D143 | Display |   |
| 52  |                           | F            | F            | F            | F            | 1            | 4            |         | Turns on the LCD for all digits (16 digits) in MDATA. |
| 53  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 54  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 55  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 56  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 57  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 58  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 59  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 60  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 61  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 62  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 63  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 64  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 65  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 66  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 67  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |
| 68  |                           | 3            | 0            | 0            | 0            | 0            | C            |         | Shifts just the MDATA display three dots to the left. |

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| No. | Instruction (hexadecimal) |              |              |              | MSB<br>D112 to D115 | Display | Operation |              |  |  |
|-----|---------------------------|--------------|--------------|--------------|---------------------|---------|-----------|--------------|--|--|
|     | D112 to D115              | D116 to D119 | D120 to D123 | D124 to D127 |                     |         |           | D128 to D131 | D132 to D135   | D136 to D139   |
| 69  |                           |              | 3            | 0            | 0                   | 0       | 0         | C            | Shifts just the MDATA display three dots to the left.  |  |
| 70  |                           |              | 3            | 0            | 0                   | 0       | 0         | C            | Shifts just the MDATA display three dots to the left.  |  |
| 71  |                           |              | 3            | 0            | 0                   | 0       | 0         | C            | Shifts just the MDATA display three dots to the left.  |  |
| 72  |                           |              | 3            | 0            | 0                   | 0       | 0         | C            | Shifts just the MDATA display three dots to the left.  |  |
| 73  |                           |              | 3            | 0            | 0                   | 0       | 0         | C            | Shifts just the MDATA display three dots to the left.  |  |
| 74  |                           |              | 3            | 0            | 0                   | 0       | 0         | C            | Shifts just the MDATA display three dots to the left.  |  |
| 75  | 0                         | 0            | 0            | 0            | 0                   | 0       | 0         | 2            | Sets AC to the DCRAM address 00H, SC to the horizontal dot address 0H and the vertical dot address 0H. |  |
| 76  |                           |              | 0            | 0            | 2                   | 0       | 0         | C            | Shifts just the MDATA display two dots to the up.  |  |
| 77  |                           |              | 0            | 0            | 2                   | 0       | 0         | C            | Shifts just the MDATA display two dots to the up.  |  |
| 78  |                           |              | 0            | 0            | 2                   | 0       | 0         | C            | Shifts just the MDATA display two dots to the up.  |  |
| 79  |                           |              | 0            | 0            | 2                   | 0       | 0         | C            | Shifts just the MDATA display two dots to the up.  |  |
| 80  |                           |              | 0            | 0            | 0                   | 0       | 0         | 8            | 4  | Sets to power saving mode, turns off the LCD for all digits.   |
| 81  |                           |              | F            | F            | F                   | F       | F         | 1            | 4  | Turns on the LCD for all digits (16 digits) in MDATA.  |
| 82  | 0                         | 0            | 0            | 0            | 0                   | 0       | 0         | 0            | 2  | Sets AC to the DCRAM address 00H, SC to the horizontal dot address 0H and the vertical dot address 0H. |



Sample 2 showing the Correspondence between Instructions and the Display (Using the LC75810-8725 with a 6 x 7 dots, 13 digits x 1 line display)

| No | Instruction (hexadecimal)                                     |              |              |              | MSB<br>D112 to D115 | Display | Operation   |
|----|---|--------------|--------------|--------------|---------------------|---------|---|
|    | D112 to D115  | D116 to D119 | D120 to D123 | D124 to D127 |                     |         |   |
| 1  | Power application<br>(initialization with the <u>RES</u> pin) |              |              |              | D136 to D139        |         | Initializes the IC.<br>The display is in the off state.   |
| 2  | Set display technique   |              |              |              | D136 to D139        |         | Sets to the 1/8 duty 1/4 bias display technique, the 32 digits x 2 lines display structure, and the 6-dot font width at each digit. |
| 3  | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "S" to DCRAM address 00H.   |
| 4  | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "A" to DCRAM address 01H.   |
| 5  | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "N" to DCRAM address 02H.   |
| 6  | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "Y" to DCRAM address 03H.   |
| 7  | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "O" to DCRAM address 04H.   |
| 8  | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data " " to DCRAM address 05H.   |
| 9  | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "L" to DCRAM address 06H.   |
| 10 | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "C" to DCRAM address 07H.   |
| 11 | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "7" to DCRAM address 08H.   |
| 12 | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "5" to DCRAM address 09H.   |
| 13 | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "8" to DCRAM address 0AH.   |
| 14 | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "1" to DCRAM address 0BH.   |
| 15 | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "0" to DCRAM address 0CH.   |
| 16 | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data " " to DCRAM address 0DH.   |
| 17 | DCRAM data write (normal increment mode)                      |              |              |              | D136 to D139        |         | Writes the display data "L" to DCRAM address 0EH.   |

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| No. | Instruction (hexadecimal)                |                       |                       |                        | MSB<br>b7401e D743 | Display | Operation   |
|-----|--|-----------------------|-----------------------|------------------------|--------------------|---------|---|
|     | LSB<br>b712 bD715 b716 bD719             | b720 bD723 b724 bD727 | b728 bD731 b732 bD735 | b736 bD739 b7401e D743 |                    |         |   |
| 18  | DCRAM data write (normal increment mode) |                       |                       |                        | 3 4                |         | Writes the display data "C" to DCRAM address 0FH. |
| 19  | DCRAM data write (normal increment mode) |                       |                       |                        | 4 4                |         | Writes the display data "D" to DCRAM address 10H. |
| 20  | DCRAM data write (normal increment mode) |                       |                       |                        | 0 2                |         | Writes the display data " " to DCRAM address 11H. |
| 21  | DCRAM data write (normal increment mode) |                       |                       |                        | 4 4                |         | Writes the display data "D" to DCRAM address 12H. |
| 22  | DCRAM data write (normal increment mode) |                       |                       |                        | 2 5                |         | Writes the display data "R" to DCRAM address 13H. |
| 23  | DCRAM data write (normal increment mode) |                       |                       |                        | 9 4                |         | Writes the display data "I" to DCRAM address 14H. |
| 24  | DCRAM data write (normal increment mode) |                       |                       |                        | 6 5                |         | Writes the display data "V" to DCRAM address 15H. |
| 25  | DCRAM data write (normal increment mode) |                       |                       |                        | 5 4                |         | Writes the display data "E" to DCRAM address 16H. |
| 26  | DCRAM data write (normal increment mode) |                       |                       |                        | 2 5                |         | Writes the display data "R" to DCRAM address 17H. |
| 27  | DCRAM data write (normal increment mode) |                       |                       |                        | 0 2                |         | Writes the display data " " to DCRAM address 18H. |
| 28  | DCRAM data write (normal increment mode) |                       |                       |                        | 0 2 0 A            |         | Writes the display data " " to DCRAM address 19H. |
| 29  | DCRAM data write (normal increment mode) |                       |                       |                        | 4 4 0 2 1 A        |         | Writes the display data "D" to DCRAM address 20H. |
| 30  | DCRAM data write (normal increment mode) |                       |                       |                        | F 4                |         | Writes the display data "O" to DCRAM address 21H. |
| 31  | DCRAM data write (normal increment mode) |                       |                       |                        | 4 5                |         | Writes the display data "T" to DCRAM address 22H. |
| 32  | DCRAM data write (normal increment mode) |                       |                       |                        | 0 2                |         | Writes the display data " " to DCRAM address 23H. |
| 33  | DCRAM data write (normal increment mode) |                       |                       |                        | D 4                |         | Writes the display data "M" to DCRAM address 24H. |
| 34  | DCRAM data write (normal increment mode) |                       |                       |                        | 1 4                |         | Writes the display data "A" to DCRAM address 25H. |

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| No. | Instruction (hexadecimal)                |      |      |      |      |      |      |      |      |      |      | MSB | Operation |  |  |      |      |      |   |
|-----|--|------|------|------|------|------|------|------|------|------|------|-----|-----------|--|--|------|------|------|---|
|     | D112 <sub>0</sub>                        | D115 | D116 | D119 | D120 | D123 | D124 | D127 | D128 | D131 | D132 |     |           | D135   | D136   | D139 | D140 | D143 |   |
| 35  | DCRAM data write (normal increment mode) |      |      |      |      |      |      |      |      |      |      | 4   | 5         | Writes the display data "T" to DCRAM address 26H.  |  |      |      |      |   |
| 36  | DCRAM data write (normal increment mode) |      |      |      |      |      |      |      |      |      |      | 2   | 5         | Writes the display data "R" to DCRAM address 27H.  |  |      |      |      |   |
| 37  | DCRAM data write (normal increment mode) |      |      |      |      |      |      |      |      |      |      | 9   | 4         | Writes the display data "I" to DCRAM address 28H.  |  |      |      |      |   |
| 38  | DCRAM data write (normal increment mode) |      |      |      |      |      |      |      |      |      |      | 8   | 5         | Writes the display data "X" to DCRAM address 29H.  |  |      |      |      |   |
| 39  | DCRAM data write (normal increment mode) |      |      |      |      |      |      |      |      |      |      | 0   | 2         | Writes the display data " " to DCRAM address 2AH.  |  |      |      |      |   |
| 40  | DCRAM data write (normal increment mode) |      |      |      |      |      |      |      |      |      |      | 0   | 2         | Writes the display data " " to DCRAM address 2BH.  |  |      |      |      |   |
| 41  | DCRAM data write (normal increment mode) |      |      |      |      |      |      |      |      |      |      | 0   | 2         | Writes the display data " " to DCRAM address 2CH.  |  |      |      |      |   |
| 42  | Set AC and SC addresses                  |      |      |      |      |      |      |      |      |      |      | 0   | 2         | Seis AC to the DCRAM address 00H, SC to the horizontal dot address 0H and the vertical dot address 0H. |  |      |      |      |   |
| 43  | Display on/off control                   |      |      |      |      |      |      |      |      |      |      | F   | 1         | 4  | Turns on the LCD for all digits (13 digits) in MDATA . |      |      |      |   |
| 44  | Display scroll                           |      |      |      |      |      |      |      |      |      |      | 3   | 0         | 0  | 0  | 1    | 1    | 4    | Shifts just the MDATA display three dots to the left. |
| 45  | Display scroll                           |      |      |      |      |      |      |      |      |      |      | 3   | 0         | 0  | 0  | 0    | 0    | C    | Shifts just the MDATA display three dots to the left. |
| 46  | Display scroll                           |      |      |      |      |      |      |      |      |      |      | 3   | 0         | 0  | 0  | 0    | 0    | C    | Shifts just the MDATA display three dots to the left. |
| 47  | Display scroll                           |      |      |      |      |      |      |      |      |      |      | 3   | 0         | 0  | 0  | 0    | 0    | C    | Shifts just the MDATA display three dots to the left. |
| 48  | Display scroll                           |      |      |      |      |      |      |      |      |      |      | 3   | 0         | 0  | 0  | 0    | 0    | C    | Shifts just the MDATA display three dots to the left. |
| 49  | Display scroll                           |      |      |      |      |      |      |      |      |      |      | 3   | 0         | 0  | 0  | 0    | 0    | C    | Shifts just the MDATA display three dots to the left. |
| 50  | Display scroll                           |      |      |      |      |      |      |      |      |      |      | 3   | 0         | 0  | 0  | 0    | 0    | C    | Shifts just the MDATA display three dots to the left. |
| 51  | Display scroll                           |      |      |      |      |      |      |      |      |      |      | 3   | 0         | 0  | 0  | 0    | 0    | C    | Shifts just the MDATA display three dots to the left. |

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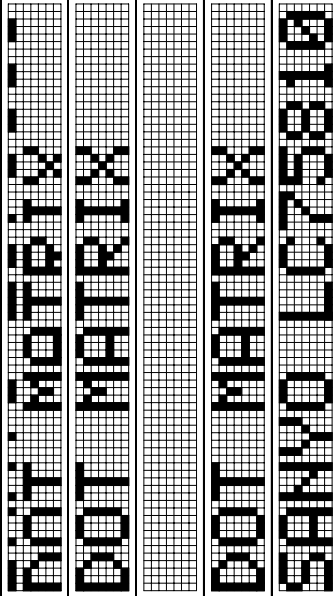
| No. | Instruction (hexadecimal) |              |              |              |              |              |              |              |         |   | MSB<br>D140 to D143 | Operation  |
|-----|---------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------|---|---------------------|--|
|     | LSB<br>D112 to D115       | D116 to D119 | D120 to D123 | D124 to D127 | D128 to D131 | D132 to D135 | D136 to D139 | D140 to D143 | Display |   |                     |  |
| 52  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 53  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 54  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 55  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 56  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 57  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 58  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 59  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 60  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 61  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 62  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 63  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 64  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 65  |                           |              | 3            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display three dots to the left.  |
| 66  | 0                         | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0       | 0 | 2                   | Sets AC to the DCRAM address 00H, SC to the horizontal dot address 0H and the vertical dot address 0H. |
| 67  |                           |              | 0            | 0            | 2            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display two dots to the up.  |
| 68  |                           |              | 0            | 0            | 2            | 0            | 0            | 0            | 0       | 0 | C                   | Shifts just the MDATA display two dots to the up.  |

Continued on next page.

Continued from preceding page.

| No. | Instruction (hexadecimal) |              |              |              |              |              |              |   |   |   | MSB | Operation  |
|-----|---------------------------|--------------|--------------|--------------|--------------|--------------|--------------|---|---|---|-----|--|
|     | D112 to D119              | D120 to D123 | D124 to D127 | D128 to D131 | D132 to D135 | D136 to D139 | D140 to D143 |   |   |   |     |  |
| 69  | Display scroll            |              |              |              |              |              |              |   |   |   | C   | Shifts just the MDATA display two dots to the up.  |
|     | 0                         | 0            | 2            | 0            | 0            | 0            | 0            |   |   |   |     |  |
| 70  | Display scroll            |              |              |              |              |              |              |   |   |   | C   | Shifts just the MDATA display two dots to the up.  |
|     | 0                         | 0            | 2            | 0            | 0            | 0            | 0            |   |   |   |     |  |
| 71  | Display on/off control    |              |              |              |              |              |              |   |   |   | 4   | Sets to power saving mode, turns off the LCD for all digits.   |
|     | 0                         | 0            | 0            | 0            | 0            | 0            | 8            |   |   |   |     |  |
| 72  | Display on/off control    |              |              |              |              |              |              |   |   |   | 4   | Turns on the LCD for all digits (13 digits) in MDATA.  |
|     | F                         | F            | F            | 1            | 1            | 1            | 4            |   |   |   |     |  |
| 73  | Set AC and SC addresses   |              |              |              |              |              |              |   |   |   | 2   | Sets AC to the DGRAM address 00H, SC to the horizontal dot address 0H and the vertical dot address 0H. |
|     | 0                         | 0            | 0            | 0            | 0            | 0            | 0            | 0 | 0 | 2 |     |  |

Display



Notes \*26: In sample 2 showing the correspondence between instructions and the display, a 13 digits × 1 line 6 × 7 dot matrix LCD is used, and CGRAM and ALATCH are not used.  
 \*27: The data format will have the following format if super-increment mode is used for the "DCRAM data write" instructions (numbers 3 to 41) in sample 2 showing the correspondence between instructions and the display.  
 Note that the sample below shows 39 characters of DCRAM data being divided into 3 separate "DCRAM data write" instruction executions in the super-increment mode.

| No.      | Instruction |            |            |             |            |            |            |            |            |            |            |            |            | MSB        |            |            |            |            |            |              |              |              |   |   |   |   |   |
|----------|-------------|------------|------------|-------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|--------------|--------------|--------------|---|---|---|---|---|
|          | LSB         |            |            | Instruction |            |            |            |            |            |            |            |            |            |            | MSB        |            |            |            |            |              |              |              |   |   |   |   |   |
|          | D24 to D27  | D28 to D31 | D32 to D35 | D36 to D39  | D40 to D43 | D44 to D47 | D48 to D51 | D52 to D55 | D56 to D59 | D60 to D63 | D64 to D67 | D68 to D71 | D72 to D75 | D76 to D79 | D80 to D83 | D84 to D87 | D88 to D91 | D92 to D95 | D96 to D99 | D100 to D103 | D104 to D107 | D108 to D111 |   |   |   |   |   |
| 3 to 15  | 3           |            |            | 5           | 1          | 4          | 4          | E          | 4          | 4          | 9          | 5          | F          | 4          | 0          | 2          | C          | 4          | 3          | 4            | 7            | 3            | 5 | 3 | 8 | 3 |   |
| 16 to 28 | 0           |            |            | 2           | C          | 4          | 4          | 3          | 4          | 4          | 4          | 4          | 0          | 2          | 4          | 4          | 2          | 5          | 9          | 4            | 4            | 6            | 5 | 5 | 4 | 2 | 5 |
| 29 to 41 | 4           |            |            | 4           | F          | 4          | 4          | 4          | 5          | 0          | 2          | D          | 4          | 4          | 1          | 4          | 4          | 5          | 2          | 5            | 9            | 4            | 8 | 5 | 0 | 2 |   |

| No.      | Instruction                             |            |            |   |            |            |            |            |            |            | MSB                                     | Operation  |            |  |            |            |            |            |            |            |            |            |              |              |              |
|----------|---|------------|------------|---|------------|------------|------------|------------|------------|------------|---|------------|------------|--|------------|------------|------------|------------|------------|------------|------------|------------|--------------|--------------|--------------|
|          | LSB                                     |            |            | Instruction                             |            |            |            |            |            |            |   |            | MSB        |  |            |            |            |            |            |            |            |            |              |              |              |
|          | D11 to D15                              | D16 to D19 | D20 to D23 | D24 to D27                              | D28 to D31 | D32 to D35 | D36 to D39 | D40 to D43 | D44 to D47 | D48 to D51 | D52 to D55                              | D56 to D59 | D60 to D63 | D64 to D67   | D68 to D71 | D72 to D75 | D76 to D79 | D80 to D83 | D84 to D87 | D88 to D91 | D92 to D95 | D96 to D99 | D100 to D103 | D104 to D107 | D108 to D111 |
| 3 to 15  | DCRAM data write (super-increment mode) |            |            | DCRAM data write (super-increment mode) |            |            |            |            |            |            | DCRAM data write (super-increment mode) |            |            | Writes the display data "S" "A" "N" "Y" "O" " " "L" "C" "7" "5" "8" "1" "0" to DCRAM addresses 00H to 0CH.   |            |            |            |            |            |            |            |            |              |              |              |
| 16 to 28 | DCRAM data write (super-increment mode) |            |            | DCRAM data write (super-increment mode) |            |            |            |            |            |            | DCRAM data write (super-increment mode) |            |            | Writes the display data " " "L" "C" "D" " " "R" " " "Y" "E" "R" " " " " " to DCRAM addresses 0DH to 19H.     |            |            |            |            |            |            |            |            |              |              |              |
| 29 to 41 | DCRAM data write (super-increment mode) |            |            | DCRAM data write (super-increment mode) |            |            |            |            |            |            | DCRAM data write (super-increment mode) |            |            | Writes the display data "D" "O" "T" " " "M" "A" "T" "R" " " "X" " " " " " " " to DCRAM addresses 20H to 2CH. |            |            |            |            |            |            |            |            |              |              |              |

LC75810-8725 Character Font (standard)

| Upper-4 bits<br>Lower-4 bits | MSB<br>0000  |     | 0001 |     | 0010 |     | 0011 |     | 0100 |     | 0101 |      | 0110 |      | 0111 |      | 1000 |   | 1001 |   | 1010 |   | 1011 |   | 1100 |   | 1101 |   | 1110 |   | 1111 |   |   |   |   |
|------------------------------|--------------|-----|------|-----|------|-----|------|-----|------|-----|------|------|------|------|------|------|------|---|------|---|------|---|------|---|------|---|------|---|------|---|------|---|---|---|---|
|                              | CG<br>RAM(1) | LSB | (2)  | (3) | (4)  | (5) | (6)  | (7) | (8)  | (9) | (10) | (11) | (12) | (13) | (14) | (15) | (16) |   |      |   |      |   |      |   |      |   |      |   |      |   |      |   |   |   |   |
| 0000                         | α            |     | 0    | !   | α    | @   | P    | p   | á    | á   | á    | á    | á    | á    | á    | á    | á    | á | á    | á | á    | á | á    | á | á    | á | á    | á | á    | á | á    |   |   |   |   |
| 0001                         | β            |     | 1    | ”   | β    | A   | Q    | q   | â    | â   | â    | â    | â    | â    | â    | â    | â    | â | â    | â | â    | â | â    | â | â    | â | â    | â | â    | â | â    |   |   |   |   |
| 0010                         | ±            |     | 2    | #   | ±    | B   | R    | r   | ê    | ê   | ê    | ê    | ê    | ê    | ê    | ê    | ê    | ê | ê    | ê | ê    | ê | ê    | ê | ê    | ê | ê    | ê | ê    | ê | ê    |   |   |   |   |
| 0011                         | ÷            |     | 3    | \$  | ÷    | C   | S    | s   | ë    | ë   | ë    | ë    | ë    | ë    | ë    | ë    | ë    | ë | ë    | ë | ë    | ë | ë    | ë | ë    | ë | ë    | ë | ë    | ë | ë    |   |   |   |   |
| 0100                         | π            |     | 4    | %   | π    | D   | T    | t   | í    | í   | í    | í    | í    | í    | í    | í    | í    | í | í    | í | í    | í | í    | í | í    | í | í    | í | í    | í | í    | í |   |   |   |
| 0101                         | ι            |     | 5    | &   | ι    | E   | U    | u   | î    | î   | î    | î    | î    | î    | î    | î    | î    | î | î    | î | î    | î | î    | î | î    | î | î    | î | î    | î | î    | î | î |   |   |
| 0110                         | Φ            |     | 6    | φ   | Φ    | F   | V    | v   | ô    | ô   | ô    | ô    | ô    | ô    | ô    | ô    | ô    | ô | ô    | ô | ô    | ô | ô    | ô | ô    | ô | ô    | ô | ô    | ô | ô    | ô | ô |   |   |
| 0111                         | φ            |     | 7    | (   | φ    | G   | W    | w   | ö    | ö   | ö    | ö    | ö    | ö    | ö    | ö    | ö    | ö | ö    | ö | ö    | ö | ö    | ö | ö    | ö | ö    | ö | ö    | ö | ö    | ö | ö |   |   |
| 1000                         | Æ            |     | 8    | )   | Æ    | H   | X    | x   | û    | û   | û    | û    | û    | û    | û    | û    | û    | û | û    | û | û    | û | û    | û | û    | û | û    | û | û    | û | û    | û | û |   |   |
| 1001                         | æ            |     | 9    | *   | æ    | I   | Y    | y   | ü    | ü   | ü    | ü    | ü    | ü    | ü    | ü    | ü    | ü | ü    | ü | ü    | ü | ü    | ü | ü    | ü | ü    | ü | ü    | ü | ü    | ü | ü | ü |   |
| 1010                         | Œ            |     | :    | +   | Œ    | J   | Z    | z   | ñ    | ñ   | ñ    | ñ    | ñ    | ñ    | ñ    | ñ    | ñ    | ñ | ñ    | ñ | ñ    | ñ | ñ    | ñ | ñ    | ñ | ñ    | ñ | ñ    | ñ | ñ    | ñ | ñ | ñ |   |
| 1011                         | œ            |     | ;    | =   | œ    | K   | [    | {   | ç    | ç   | ç    | ç    | ç    | ç    | ç    | ç    | ç    | ç | ç    | ç | ç    | ç | ç    | ç | ç    | ç | ç    | ç | ç    | ç | ç    | ç | ç | ç | ç |
| 1100                         | →            |     | <    | ←   | →    | L   | ¥    |     | š    | š   | š    | š    | š    | š    | š    | š    | š    | š | š    | š | š    | š | š    | š | š    | š | š    | š | š    | š | š    | š | š | š | š |
| 1101                         | ←            |     | =    | →   | ←    | M   | ]    | }   | ş    | ş   | ş    | ş    | ş    | ş    | ş    | ş    | ş    | ş | ş    | ş | ş    | ş | ş    | ş | ş    | ş | ş    | ş | ş    | ş | ş    | ş | ş | ş | ş |
| 1110                         | ↑            |     | >    | ·   | ↑    | N   | ^    | —   | ğ    | ğ   | ğ    | ğ    | ğ    | ğ    | ğ    | ğ    | ğ    | ğ | ğ    | ğ | ğ    | ğ | ğ    | ğ | ğ    | ğ | ğ    | ğ | ğ    | ğ | ğ    | ğ | ğ | ğ | ğ |
| 1111                         | ↓            |     | ?    | /   | ↓    | O   | _    | ■   | i    | i   | i    | i    | i    | i    | i    | i    | i    | i | i    | i | i    | i | i    | i | i    | i | i    | i | i    | i | i    | i | i | i |   |

# LC75810E, LC75810T

## Package Dimensions

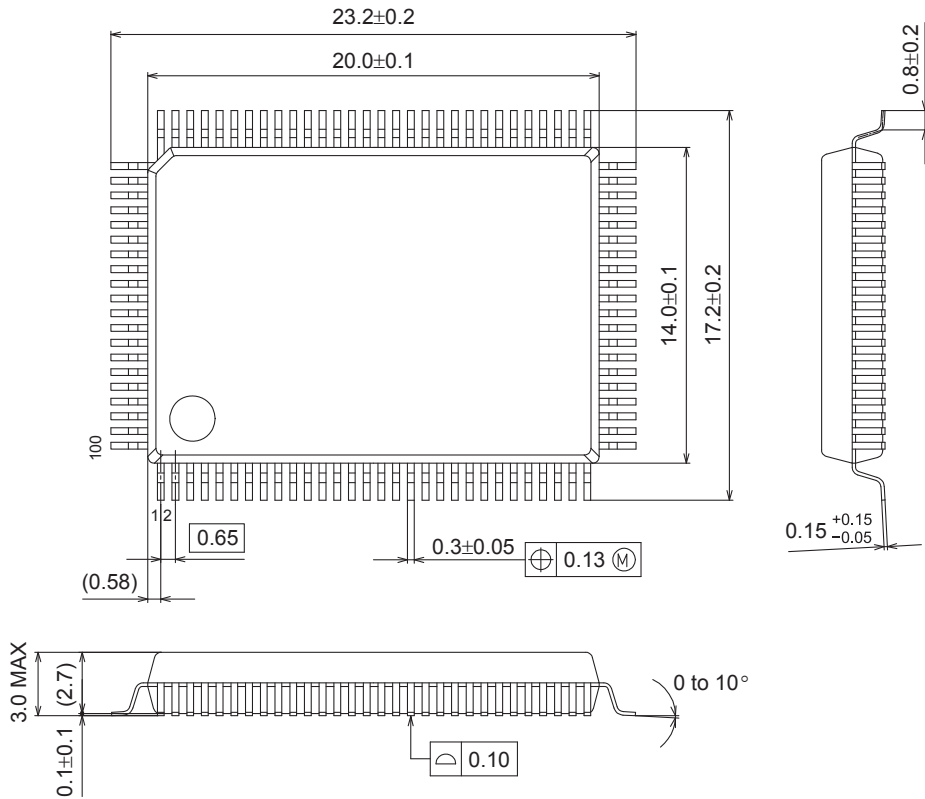
unit : mm

[LC75810E]

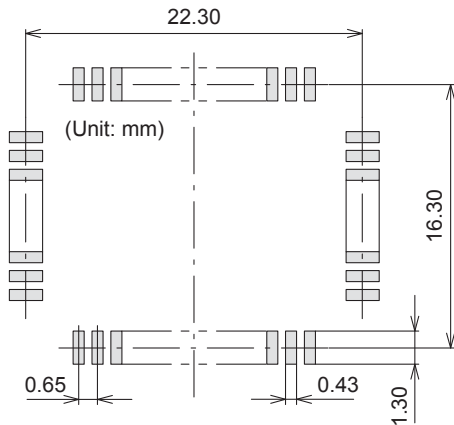
PQFP100 14x20 / QIP100E

CASE 122BV

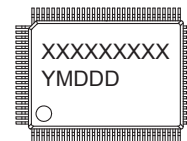
ISSUE A



### SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
 Y = Year  
 M = Month  
 DDD = Additional Traceability Data

NOTE: The measurements are not to guarantee but for reference only.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic.  
 Pb-Free indicator, "G" or microdot "•", may or may not be present.

# LC75810E, LC75810T

## Package Dimensions

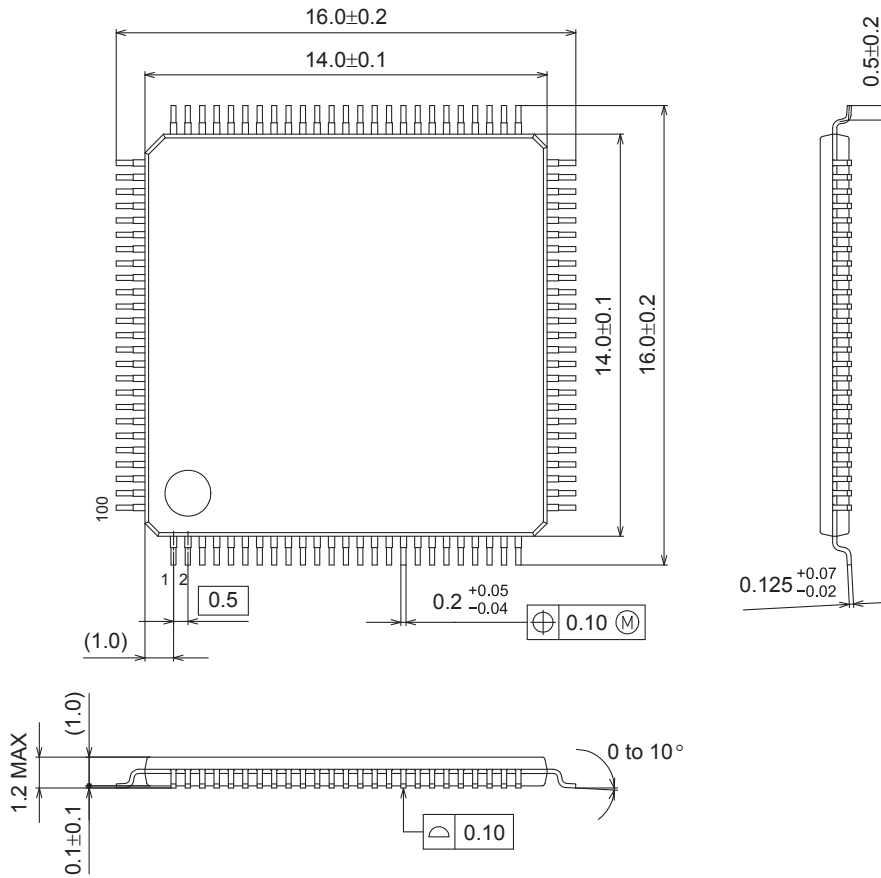
unit : mm

[LC75810T]

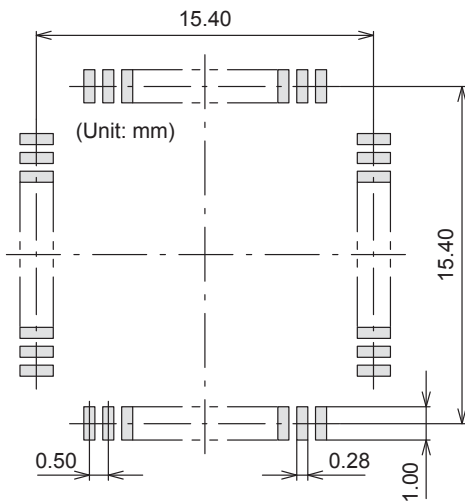
### TQFP100 14x14 / TQFP100

CASE 932AY

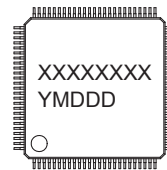
ISSUE A



### SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
Y = Year  
M = Month  
DDD = Additional Traceability Data

\*This information is generic.  
Pb-Free indicator, "G" or microdot "■", may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## LC75810E, LC75810T

### ORDERING INFORMATION

| Device           | Package                              | Shipping (Qty / Packing) |
|------------------|--------------------------------------|--------------------------|
| LC75810E-8725-E  | PQFP100 14x20 / QIP100E<br>(Pb-Free) | 250 / Tray Foam          |
| LC75810T-8725-E  | TQFP100 14x14 / TQFP100<br>(Pb-Free) | 450 / Tray JEDEC         |
| LC75810TS-8725-E | TQFP100 14x14 / TQFP100<br>(Pb-Free) | 90 / Tray JEDEC          |

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